Layout Tutorial for Lab 3: Automated Design, Synthesis, and Layout

We won't be doing the layout of each cell ourselves. Instead we will be using "black box cells". The black boxes are provided by CMC and TSMC (CMC provides access to the materials and TSMCs fabrication facility). The black box cells are place holders (look them up in the library manager when you get the chance) and will be filled in by CMC when the design is submitted for fabrication (something we wont be doing). Instead we are going to use Encounter (a cadence tool) to do the following:

- Floor planning,
- Place and route,
- Power distribution
- Clock distribution.

Once we are done we will have a prototype layout for our Verilog module that can be sent to CMC for fabrication (once they replace the black boxes with the real cells).

The layout lab is a continuation of the synthesis work you did last week. Therefore, we will need the synthesised version of your signed serial multiplier. This example will use the synthesized counter from the previous tutorial.

Make sure you have a saved copy of your synthesized module (if necessary run design analyzer again). It is best to save a version of your synthesized module in a separate directory.

- Open a terminal console, go to your lab2 directory, and create a constraint file. You may have to change "Clk" to the name of your Clock pin, and "Reset" to the name of your Reset pin. >cd elec4708s
 - >cd lab2

>echo -e "set_time_unit -nanoseconds\ncreate_clock -name {Clk} -period 10.0
-waveform {0.0 5.0} [get_ports {Clk}]\nset_false_path -from [get_ports
{Reset}]" > constraint.sdc

2. Now create a Clock specification file. You may have to Change "Clk" to the name of your Clock pin.

>echo -e "AutoCTSRootPin Clk \nBuffer CKBD1 CKBD8 CKBD16 CKBD20 CKBD24 \nEND" > Clock.ctstch

 Now we want to save a copy of your synthesized module in a new directory but first we need to make a directory to save it to.
 >mkdir synthesized

Now we need to run design analyzer as before (see tutorial for part 2 of lab 3. Make sure your in the right directory) and add a new step at the end as follows:

4. Go back to the top level of the hierarchy. Save the design using File-->Save As. Save the file in the "Synthesized" directory with file name "counter.v". Make sure you save it with the VERILOG format, and save the full hierarchy.

Save Design As	×
Look in: Sukneetbasuta/elec4708/tut2/FE/synthesized/ 💌 💠 f	1 💣 🧱 🇰
File <u>n</u> ame: counter	<u>S</u> ave
File type: Database Files (*.ddc *.ddc.gz *.db *.db.gz *.gdb *.	Cancel
Eormat: VERILOG (v)	SYNOPSYS'
Save all designs in hierarchy	1.

 Now we can start encounter. In a terminal console make sure that you are in the lab2 directory and type >encounter

Encounter(R)	RTL-to-GDSII System 11.2	12 - /home/sukneetbasuta/e	lec4708/tut2/FE -	_ = ×
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Click to select single object. Shift+Click to) de/select multiple objects.	Q	SelNum:0 (0.062, -0.229)	Not in Memory

6. In encounter we now need to import the design that we saved in the synthesized directory. Go to File -> Design Import, and fill in the pop-up window as shown below (modify the file locations to suit where your files are saved). Set VDD as the Power net, and VSS as the ground net.

Use the following path for the LEF Files:

/CMC/kits/tsmc_65nm_libs/tcbn65gplus_200a/TSMCHOME/digital/Back_End/le
f/tcbn65gplus_200a/lef/tcbn65gplus_91mT2.lef

	Design Import _ 🗆
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● Verilog	
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O OA	
Library:	
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Technology/Physical Libr	raries:
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Reference Libraries:	
Abstract View Names:	
Layout View Names:	
LEF Files	HOME/digital/Back_End/lef/tcbn65gplus_200a/lef/tcbn65gplus_9ImT2.lef
Floorplan	
IO Assignment File:	
Power	
Power Nets:	VDD
Ground Nets:	VSS
CPF File:	
Analysis Configuration —	
MMMC View Definition File	a: 🖻 🖻
	Create Analysis Configuration
	Save Load Cancel Help

Hit OK.

7. Now lets specific the timing libraries. Select **Timing->Configure MMMC**. The MMMC browser window will popup.

MMMC Bro	wser _ 🗆 X
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Analysis Views - Analysis Views - Setup Analysis Views - Hold Analysis Views	MMMC Objects
OK Save Load Delete Reset	Preferences Wizard On <u>C</u> lose <u>H</u> elp

Double click on "Library Sets" at the top. A window asking for a library set should popup.

	Add Library	/ Set	_ = ×
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	Add		Add
	Delete		Delete
<u><u>o</u>k</u>	<u>A</u> pply	Close	<u>H</u> elp

Hit the "Add" button under the Timing Library Files section. Add the following path: /CMC/kits/tsmc_65nm_libs/tcbn65gplus_200a/TSMCHOME/digital/Front_End/t iming_power_noise/NLDM/tcbn65gplus_140b/tcbn65gpluswc.lib

Tim	ing Library Files	×
Timing Library File:	cbn65gpluswc.lib	
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/CMC/kits/tsmc_6	5nm_libs/tcbn65gplus_200a/TSN	
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	Close	

Add the library and hit close.

Give the library set a name (let's call it "worst_case" since we are using the worst case timing library) and Hit Ok.

	Add Library	/ Set	_ 🗆 X
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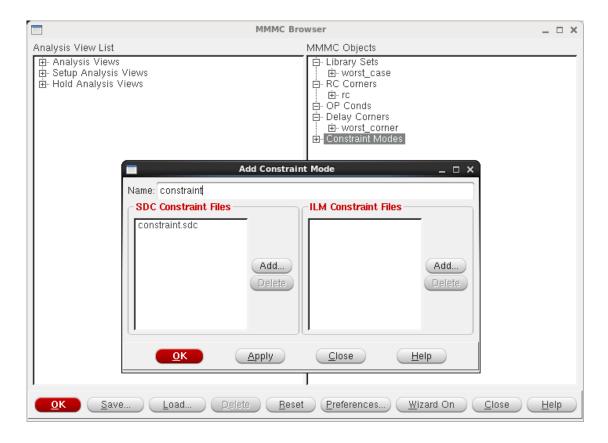
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	PreRoute Clock Resistance Scale Fact	tor: 0.0
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Next double click on **RC Corners**, set a Temperature of 25, and give it a name. Hit Ok.

Double click on **Delay Corners**, set the RC Corner to the one you just defined and the library set to the library you defined earlier, and give it a name. Hit Ok.

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		Attributes	
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	Add	Library Set:	
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		IrDrop File:	
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	<u>A</u> pply	<u>Close</u> <u>Help</u> se	Help

Double click on **Constraint Modes**, add the constraint file you created in Step 1, and give it a name. Hit Ok.



Double Click on **Analysis Views** and give it a name. Hit Ok.

	MMMC Browser	_ = ×
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Analysis View List	MMMC Objects	
<u>OK</u> <u>S</u> ave	Load Delete Reset Preferences Wizard On Close (<u>H</u> elp

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Analysis View List	 MMMC Objects
, <u>OK</u> <u>Save</u> <u>Load</u> <u>Delete</u> <u>R</u> eset	Preferences) Wizard On Close Help

Double click on **Setup Analysis Views** and select the analysis view you just created. Hit OK.

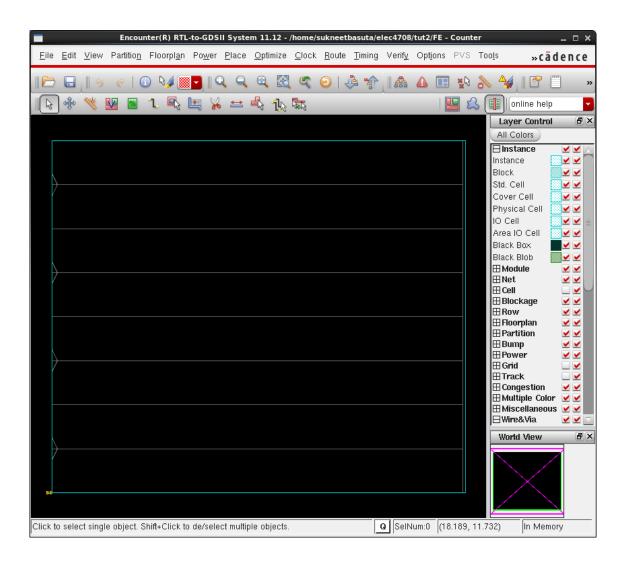
Double click on Hold Analysis Views and select the analysis view you just created. Hit OK.

	MMMC Browser	– – ×
Analysis View List	MMMC Objects	
 Analysis Views ⊕- worst_analysis ⊡- Setup Analysis Views ⊕- worst_analysis ⊕- Hold Analysis Views 	i⇔- Library Sets i⊕- worst_case i⊕- RC Corners i⊕- rc i⊕- OP Conds i⊕- Delay Corners i⊕- worst_corner i⊕- Constraint Modes i⊕- constraint	
	Add Hold Analysis View _ C × Analysis View: worst_analysis OK Apply Close Help	
OK Save	Load Delete Reset Preferences Wizard On Close	<u>H</u> elp

Hit **OK** on the MMMC browser window.

8. We can now see the initial floor plan (you may have to zoom out with **View->Fit** or with the

Zoom fit subtraction on the top toolbar) and the module in the bottom left of the window (the counter is very small and doesn't take up much room in the module view).



9. The next step is to specify the floor plan. We need to leave enough space so that the router will be able to place all the metal interconnects, but not so much that we waste space. We also want to have a large enough space for any buffers that might be needed during optimization. A decent number for core utilization is somewhere between 0.5 and 0.7 (The default is most likely fine).

We also need to decide how much space we want to leave around the core. Keep in mind that we want to add our power rings so we might need something like 15 - 50 microns of space (for the counter we will use 20 microns). From the encounter window select **Floorplan-> Specify Floorplan**.

Specify Floo	orplan	
asic Advanced		
Design Dimensions		
Specify By: 💿 Size 🔾 Die/IO/Core	Coordinates	
🖲 Core Size by: 🖲 Aspect Ratio	: Ratio (H/W):	561134082
	Core Utilization:	0.699941
	Cell Utilization:	0.699941
Dimension:	Width:	16.93
	Height:	14.4
🔾 Die Size by:	Width:	16.93
	Height:	14.4
Core Margins by: 💽 Core to IO B	oundary	
Core to Die	Boundary	
Core to Left:	20 Core to Top:	20
Core to Right:	20 Core to Bottom:	20
Die Size Calculation Use: 🔾 Ma	x IO Height 🧕 Min I	O Height
Floorplan Origin at: 🛛 💿 Low	er Left Corner 🔾 Cen	ter
		Unit: Mic

After you click "OK", the encounter window should now look like this

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We can see that the chip has been divided into three sections. You can play around with some of the Floorplan numbers to get different sizes, size ratios, core boundary sizes, etc.

Now is probably a good time to save your work. It's also probably a good idea to save often.
 Select the File -> Save Design. Save your design with the Encounter Data Type (OA doesn't restore properly). You can restore a saved design by selecting File-> Restore Design. When you

restore the design, you may have to select the physical view button in the top toolbar. You can save your layout in your lab2 library with view layout so you can run simulations with it later in Cadence if you wish. If that doesn't work, select Encounter.

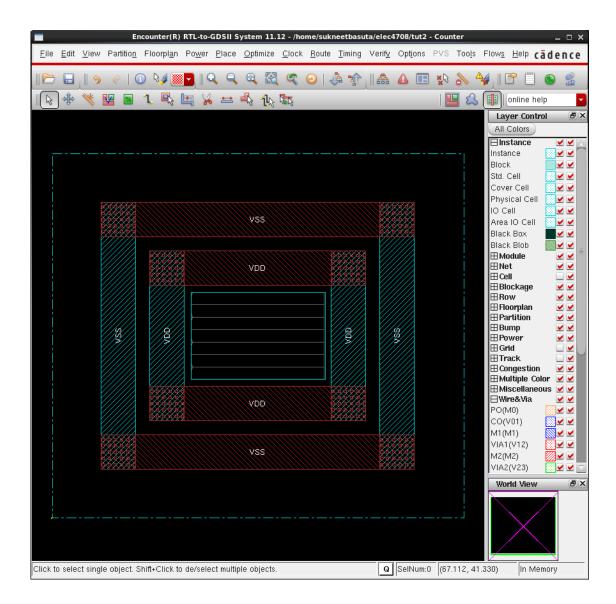
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11. We can now add the power rings around the core. Select **Power->Power Planning -> Add Ring...**

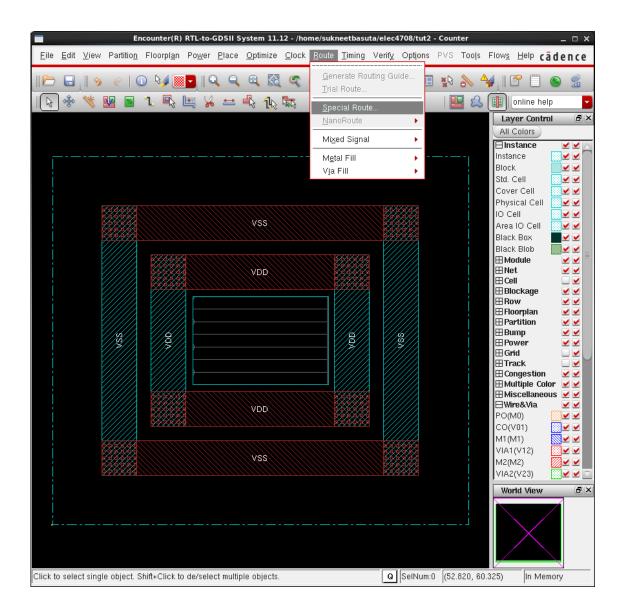
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12. Select the VDD and VSS Nets by clicking on the "…" button. Make the power lines 5 microns wide and use Metal 9 for top and bottom and metal8 for left and right. Click on "Update". Set an offset of 1 micron. Click "OK". The width of the power lines is determined (somewhat) by the size of the chip. A much bigger design would need wider lines.

Ring Type					
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Around core		🔾 Along I	/O boundary		
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	1	· · ·	1		
1	<u> </u>	1	1		
Option Set ——					
Edit Add Ring	Option				



13. Now we need to add the power routing. Select Route -> Special Route



14. In the SRoute window, select the VDD and VSS nets by clicking on the "..." button. The rest of the defaults should be fine.

Net(s): VDD VSS			
SRoute			
💆 Block Pins 💆 Pad Pins	🗹 Pad Rings 🗹 Follow Pins 🔲 Second:	ary Power Pins	
Routing Control			
Layer Change Control			
Top Layer: 🛛 AP 🕨	Bottom Layer: M1 🕨		
🗹 Allow Jogging	🗹 Allow Layer Change		
🗌 Area		Power Domain Selection	
X1:	Y1: Draw	 All Selected 	
X2: Connect to Target In	Y2: View Area	O Named:	
Delete Existing Routes	side The Area Only		
Generate Progress Mess	ages		
📃 Extra Config File:	Ex (Ex	tra Config Editing	
			Target Editing Option

When it's done, your layout should look similar to the layout below. There are alternating power stripes between the power rings.

Elle Edit View Partition Floorplan Power Place Optimize Clock Boute Timing Verify Options PVS Tools Flove Help Câdence
Image: Section of the section of th
Image: Control Image
VIA2(V23) ✓ ✓ World View ✓ Click to select single object. Shift+Click to de/select multiple objects. Q SelNum:0 (91.272, 43.912) In Memory

15. Now that we have routed our power wires, we need to define global net connections so that that power planning, power routing, detail routing, and power analysis function work correctly.

Select **Power -> Connect Global Nets**. The Global Net Connections window will popup We want to add the following connections:

- Pin VDD -> Global Net VDD
- Pin VSS -> Global Net VSS
- TIEHI -> Global Net VDD
- TIELO -> Global Net VSS

Fill in the VDD connection like the following and do the same for VSS:

	Global Net Connections	_ o x
Connection List	Power Ground Connection	
	Connect	
	● Pin	
	🔾 🔾 Tie High	
	🔾 Tie Low	
	Instance Basename: *	
	Pin Name(s): VDD	
	🔾 Net Basename:	
	C Scope	
\odot	Single Instance:	
	Under Module:	
•	Under Power Domain:	
	Under Region: IIx: 0.0 IIy: 0.0 urx: 0.0	ury: 0.0 🎽
	Apply All	
	To Global Net: VDD	
	Override prior connection	
	Uerbose Output	
	Add to List Update	Delete
Apply Ch	<u>Bok</u> <u>R</u> eset <u>C</u> ancel	Help

	Global Net Connections	_ = ×
Connection List	Power Ground Connection	
Connection List VDD:PIN:*.VDD:All VSS:PIN:*.VSS:All VD:TIEHI:*.:All VSS:TIELO:*.:All	Power Ground Connection Connect Pin Tie High Tie Low Instance Basename: Pin Name(s): Net Basename: Scope Single Instance: Under Module: Under Power Domain: Under Region: Instance Instance Onder Region: Instance Instance <th>ury: 0.0</th>	ury: 0.0
	Apply All To Global Net: VSS Override prior connection Verbose Output Add to List Update	Delete
Apply	iheck <u>R</u> eset <u>Cancel</u>	Help

The TIEHI and TIELO connections are done like the following:

Once done, Hit Apply and close the window.

16. We can now place our cells. Select **Place -> Place Standard Cell...**

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Click to select si	ngle object. S	Shift+Click to	o de/sele	ct multiple objects				Q	SelNum:	0 (35.	853,60.	510)	In N	1emory	
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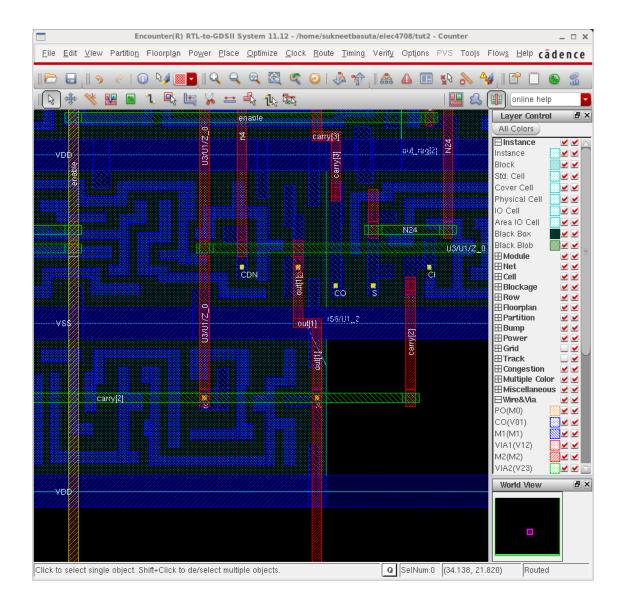
Place _ 🗆 X
🖲 Run Full Placement 🔾 Run Incremental Placement 🔾 Run Placement In Floorplan Mode
Optimization Options
✓ Include Pre-Place Optimization □ Include In-Place Optimization
Number of Local CPU(s): 1 Set Multiple CPU
<u>OK</u> <u>Apply</u> <u>Mode</u> <u>Defaults</u> <u>Cancel</u> <u>H</u> elp

17. If you do not see the standard cells, you can zoom in and out with the mouse wheel, which will refresh the view. You can see that the input and out pins were added wherever routing was

convenient. If you want to specify the location of the pins, you can change them by selecting Edit->Pin Editor. We do not have specifications for the pin locations, so we will leave them where they are.

Elle gelt View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options PVS Tools Flows Help câdence	Enc	ounter(R) RTL-to-GDSII Sy	stem 11.12 - /home/s	sukneetbasuta/ele	ec4708/tut2 - Cou	unter	_ 🗆 X
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User Control Imstance VSS Imstance VSS VSS VDD Std. Cell Std. Cell Std. Std. Cell Std. Cell Std. Std. Cell Std. Std. Cell Std. Std. Std. Std. Std. Std. Std. Std.	🎦 🗔 🛛 🥱 🦿 🗊	· №ø 💽 I Q. Q.	् 🔣 ⊄ 📀		A 🔝 🔛	3 🏡 🐳 🛛 🕾	🗒 🛞 🔒
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VIA2(V23)			VSS VDD Sours 6 d dut real sours 6 d d dut real sours 6 d d d d d d d d d d d d d d d d d d			Layer All Col Dinstau Instance Block Std. Cel Cover C Physica IO Cell Area IO Black B Black Bl	Control Image Ors Ince Image Image Image

If you zoom in, you may notice that you cannot see inside the cells. If you Check the first checkbox for **Cell** under layer Control on the right, you can see inside the cells.



18. Now we need to insert a clock tree. We already created the specification file in Step 2. It is possible to generate the specification file by clicking on Gen Spec in the Synthesize Clock Tree window and selecting the proper buffers. However you still need to specify the Clk pin the generated file, so it is easiest to use the one in Step 2.

Select Clock-> Synthesize Clock Tree.

	Encounter(R) RTL-t	o-GDSII System 11.12	- Counter.enc.dat	- Counter	×
<u>F</u> ile <u>E</u> dit <u>V</u> iew Partitio <u>n</u>	Floorpl <u>a</u> n Po <u>w</u> er <u>P</u> lace	<u>O</u> ptimize <u>C</u> lock <u>R</u> ou	te <u>T</u> iming Verify	<u>≀</u> Opt <u>i</u> ons PVS	Tools Flows Help cadence
∥ ि ि ,∥ >) ﴾ ≢ ∭ <mark>.</mark> Q Q 1	Tr <u>a</u> ce Pro Browse C Debug C Display	ze Clock Tree e-CTS Clock Tree. Clock Tree lock Tree		Image: Second
		Sa <u>v</u> e Clo <u>G</u> enerate	ck Net Clock Tree Spice		Instance ⊻ ⊻ ∧ Instance ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■
		<u></u> lock Me		•	Block Std. Cell Cover Cell
		Report SI	DC Clock Definitio	n	Physical Cell 🛛 🗹 🗹 IO Cell 🔅 🗹 🗹 Area IO Cell 🔅 🗹 🗹 Black Box 🔤 🗹 🗸
		VDD			Black Blob ✓ ✓ ■ ⊞ Module ✓ ✓ ■ ⊞ Net ✓ ✓ ⊞ Cell ✓ ✓ ✓ ⊞ Blockage ✓ ✓
	opt, reality r5	56/U1_5 6/U1_5 6/U1_5 6/U1_5 6//U1_6			
		ut_reg(3) -043 -rec(4) 155/01 11 -rut reg(2) 155/01 21 -rut reg(2)			■ Bump ■ ♥ ♥ ■ Power ■ ♥ ■ Grid ■ ♥ ■ Track ■ ♥
	r56/UI 0 s T	567U 11 13:			 ⊞ Congestion ✓ ✓ ✓ ⊞ Multiple Color ✓ ✓ ⊞ Miscellaneous ✓ ✓
		VDD			₩ire&Via ⊻ PO(M0) 2 ⊻ CO(V01) 2 ⊻
		vss			M1(M1)
Click to select single object. S	hift+Click to de/select multin	e objects		SelNum:0 (51.)	World View B ×

The Synthesize Clock Tree window should popup. Set the Clock Specification file to "Clock.ctstch". The rest of the defaults should be fine. Hit OK and look at the terminal to determine if it was successful.

Synthesize Clock Tree	_ 🗆 X
Basic Advanced	
Clock Specification Files: Clock.ctstch Gen Spec	
Results Directory: clock_report	
<u>OK</u> <u>Apply</u> <u>Mode</u> Loa <u>d</u> Spec <u>Cl</u> ear Spec <u>C</u> ancel	<u>H</u> elp

19. Placing the standard cells automatically routed the wires for the standard cells for us, but to ensure everything is routed lets use Nanoroute. Select **Route-> Nanoroute -> Route**

Eile Edit View Partition	counter(R) RTL-to-GDSII : Floorpl <u>a</u> n Po <u>w</u> er <u>P</u> lace					Flow <u>s</u> <u>H</u> elp ca	_□× dence
) V/ 💓 🛛 IQ Q 1 🖳 🖭 🏑 🖴	 Q Q Q Q Q Q Q Q Q Q Q Q Q Q Q Q Q Q Q <lp>Q </lp> <	Generate Routi Trial Route Special Route. NanoRoute Mixed Signal Metal Fill			nce	
		vss	V <u>i</u> a Fill			Block Std. Cell Cover Cell Physical Cell IO Cell Area IO Cell Black Blob El Module	
						 Het ⊞ Cell ⊞ Blockage ⊞ Row ⊞ Floorplan ⊞ Partition ⊞ Bump ⊞ Power ⊞ Grid ⊞ Track 	L KKKKKK K K K K K K K K C
		VDD VSS					
Click to select single object. S	hift+Click to de/select multi	ple objects.		Q SelNum:0	(47.564, 59	VIA2(V23) World View 404) Routed	

20. Use the default values for NanoRoute and hit OK. All your wires should be routed now.

Routing Phase Global Route Detail Route Start Iteration default Post Route Optimization Optimize Via Optimization Optimize Via Optimize Via Optimize Wire Concurrent Routing Features Fix Antenna Fix Antenna Insert Diodes Diode Cell Name Timing Driven Effort 5 SI Driven Congestion Timing Post Route SI SI Victim File SI MA.R.T. SI Driven SI Victim File SI MA.R.T. Utho Driven SI Victim File SI SI Victim File Utho Driven Selected Nets Only Bottom Layer default Top Layer default ECO Route Area Route Area Select Area and Route Job Control Mumber of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine: Number of Remote Machine: Number of CPU Set Multiple CPU		NanoRoute _ 🗆 X
 ✓ Fix Antenna Insert Diodes Diode Cell Name Timing Driven Effort 5 Congestion Timing S.M.A.R.T. SI Driven Post Route SI SI Victim File Litho Driven Post Route Litho Repair Routing Control Selected Nets Only Bottom Layer default Top Layer default ECO Route Area Route Area Select Area and Route Job Control Victim File Victim File ECO Route Area Route Area Select Area and Route Job Control Victim File Victim File Victim File Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0 	 ✓ Global Route ✓ Detail Route ✓ Detail Route 	
□ Timing Driven Effort 5 Congestion Timing S.M.A.R.T. □ SI Driven □ SI Victim File □ Post Route SI SI Victim File □ □ Litho Driven □ □ □ Post Route Litho Repair □ □ Routing Control □ □ □ Selected Nets Only Bottom Layer default Top Layer default □ ECO Route □ Select Area and Route Job Control □ Select Area and Route ✓ Auto Stop Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine: 1 Number of Remote Machine: 5: 0 □	- Concurrent Routing Featu	res
□ Timing Driven Effort 5 S.M.A.R.T. □ SI Driven □ S.M.A.R.T. □ Post Route SI SI Victim File □ □ Litho Driven □ □ □ Post Route Litho Repair □ □ Routing Control □ □ □ Selected Nets Only Bottom Layer default Top Layer default □ ECO Route □ Select Area and Route Job Control ☑ Auto Stop □ Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0 □	🗹 Fix Antenna	Insert Diodes Diode Cell Name
 Post Route SI SI Victim File Litho Driven Post Route Litho Repair Routing Control Selected Nets Only Bottom Layer default Top Layer default ECO Route Area Route Area Job Control Value Stop Number of Local CPU(s): 1 Number of Remote Machine: 1 Number of Remote Machine(s): 0 	Timing Driven	Effort 5 SMART
 Litho Driven Post Route Litho Repair Routing Control Selected Nets Only Bottom Layer default Top Layer default ECO Route Area Route Area Select Area and Route Job Control ✓ Auto Stop Number of Local CPU(s): 1 Number of Remote Machine: 1 Number of Remote Machine(s): 0 	🔲 SI Driven	
 Post Route Litho Repair Routing Control Selected Nets Only Bottom Layer default Top Layer default ECO Route Area Route Area Select Area and Route Job Control Number of Local CPU(s): 1 Number of Remote Machine: 1 Number of Remote Machine(s): 0 	Post Route SI	SI Victim File 📄
Routing Control Selected Nets Only Bottom Layer default Top Layer default ECO Route Area Route Area Select Area and Route Job Control ✓ Auto Stop Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0	🔲 Litho Driven	
 Selected Nets Only Bottom Layer default Top Layer default ECO Route Area Route Area Select Area and Route Job Control ✓ Auto Stop Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0 	🔲 Post Route Litho Repair	
 ■ ECO Route ■ Area Route Area Select Area and Route Job Control ✓ Auto Stop Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0 	- Routing Control	
 □ Area Route Area → Select Area and Route → Job Control ✓ Auto Stop Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0 	Selected Nets Only	Bottom Layer default Top Layer default
Job Control ✓ Auto Stop Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0	ECO Route	
 ✓ Auto Stop Number of Local CPU(s): 1 Number of CPU(s) per Remote Machine: 1 Number of Remote Machine(s): 0 	🔲 Area Route 🛛 Area	Select Area and Route
OK Apply Attribute Mode Save Load Close Help	✓ Auto Stop Number of L Number of CPU(s) per Remove Number of Remote Set Multiple CPU	ote Machine(s): 0

21. We can now do a timing optimization. Select **Optimize -> Optimize Design**

Enc	ounter(R) RTL-to	GDSII System 11.12 -	/home/sukneetbas	uta/elec4708/tut	2 - Counter	_ = ×
<u>F</u> ile <u>E</u> dit <u>V</u> iew Partitio <u>n</u> P	Floorpl <u>a</u> n Po <u>w</u> er	<u>P</u> lace <u>O</u> ptimize <u>C</u> lo	ock <u>R</u> oute <u>T</u> iming	Verif <u>y</u> Opt <u>i</u> ons	PVS Too <u>i</u> s	Flow <u>s</u> <u>H</u> elp cādence
	₽₫ 💹 🗖	Q Q Optimize N	etlist 🔥 ᆎ	A 🔒 🔳	1 🖏 🝌 4	¥ I 🖀 🗒 🖌
	ι 🗈 🖭 🖌	O <u>p</u> timize D	esign			online help
	0 0	<u>Interactive</u>				Layer Control
		Display No	ISE NEL			All Colors
						Instance 🛛 🗹 🗹 🗂
						Block 🖉 🗹 🗹 Std. Cell
						Cover Cell 🛛 🗹 🗹 Physical Cell 🔍 🗹 🗹
						IO Cell 🔤 🗹 🗹
		vss				Black Box 📃 🗹 🗹
						Black Blob ✓ ✓ ⊞ Module ✓ ✓
						⊞Net ⊻⊻ ⊞Cell ⊻
		VDD				⊞ Blockage ⊻ ⊻ ⊞ Row ⊻ ⊻
		15 6/U1_5				⊞ Floorplan ✓ ✓ ■ Partition
			t rea(5 /U1 4			⊞ Bump ⊻ ⊻ ⊞ Power ⊻ ⊻
			ADDRESS ADDRESS AND ADDRESS ADDRE			⊞ Grid ⊞ Track
			it re 1121			🖽 Congestion 🛛 🗹 🗹
		1997 - 19				Hultiple Color ⊻ ⊻ Miscellaneous ⊻ ⊻
						⊟Wire&Via ⊻ ⊻ PO(M0) ∑ ⊻
						CO(V01)
						VIA1(V12)
		vss 🛛				VIA2(V23)
						World View
Click to select single object. Sh	ift+Click to de/sel	ect multiple objects.		Q SelNum	:0 (32.852, 63	3.806) Routed

In the Optimization window, select "Post-Route" and Hit Ok.

	Optimi	zation	_ o x
- Design Stage -]
O Pre-CTS	O Post-CTS	Post-Route	◯ Sign-Off
Optimization T	ype		
🗹 Setup		Hold	
🔾 Incremental			
Design Rules	s Violations		
🗹 Max Cap			
🗹 Max Tran			
📃 Max Fanou	ıt		
🗌 🗆 Include SI 🌘	SI Options)		
	pply <u>M</u> ode	<u> </u>	<u>Close H</u> elp

It will be difficult to see any changes in the layout so check the terminal window which should show a summery of changes

22. Now that we have routed all the wires and placed all the cells we require, we will add empty filler cells to the design. Select **Place -> Physical Cell -> Add Filler**

		ll System 11.12 - /hom					_ 0 X
<u>F</u> ile <u>E</u> dit <u>V</u> iew Partitio <u>n</u> F	loorpl <u>a</u> n Po <u>w</u> er <u>P</u> la	ce <u>O</u> ptimize <u>C</u> lock	<u>R</u> oute <u>T</u> iming V	'erif <u>y</u> Opt <u>i</u> ons	PVS Too <u>i</u> s	Flow <u>s</u> <u>H</u> elp ca	dence
ि 🕞 🥱 🔗 ①	₽∌ 💽 🛛 🖕	Specify	🕭 🏫	A 💧 🔳	👷 💦 🐴	/ 1 🖀 🗍	۵
🛛 🖓 🚸 💘 🕎 🖬 1	. 🖳 📺 🔏	Place <u>J</u> tag Place Stand <u>a</u> rd Cell			1 🔛 🕰	online help) 🔽
		Place Spare Cell				Layer Contro	I ð×
		<u>R</u> efine Placement				All Colors	
	_ النصناط	ECO Placement				Instance	<u> </u>
		Physical Cell	Add <u>W</u> ell Tap	 D		Block Std. Cell	
		Scan Chain	- Add <u>E</u> nd Cap Add Filler)		Cover Cell Physical Cell	¥ ¥ ¥ ¥
		Check Placement	<u>D</u> elete Filler			IO Cell Area IO Cell	× ×
		Display	Add I/O Fille	r		Black Box	
		Query Density	Delete I/O Fi	ller		Black Blob Module	
		VUD	<u>C</u> heck Filler			⊞ Net ⊞ Cell	¥ ¥
						⊞ Blockage ⊞ Row	× ×
	out realt	ii. Habilii ee e 🖬 🚽 tare(⊞ Floorplan ⊞ Partition	⊻ ⊻
T/2///		n in a star grad req	P1 //9///		ť	⊞ Bump	žž
		in 1567 an dis sei tale rei See ta concelle dis an availability	2			⊞ Power ⊞ Grid	Ľ≚_
T		500 11 COLD 210 00 52 272 5300 50 2000 000 000 000 50 11 02745 1505 50				⊞Track ⊞Congestion	× ×
i /////						⊞ Multiple Colo ⊞ Miscellaneou	
i /////						⊟Wire&Via PO(M0)	
						CO(V01)	× ×
		vss 👘				M1(M1) VIA1(V12)	× × × ×
8539999				10000000		M2(M2) VIA2(V23)	፼ ⊻ ⊻ ▼ ▼ ▼
						World View	6 ×
							7
Click to coloct single object. Child	t. Click to do (sola at m	ultiple chiects		O Salklum	/26.248 00	100) Timin a	Analuzari
Click to select single object. Shif	t+Click to de/select mi	umple objects.			(26.248, 60.	i sə) li iming	Analyzed

In the Add Filler window, select the DCAP and FILL1 cells and check of Mark Fixed. DCAP places a capacitor between VDD and VSS.

Add Filler	_ 🗆 X
Cell Name(s) DCAP FILL1	Select
Prefix FILLER	
Power Domain	Select
 No DRC Mark Fixed Fill Area Draw View Area 	
lix liy	
urx ury	
<u>O</u> K <u>A</u> pply <u>M</u> ode <u>C</u> ancel	Help

After you hit OK, you will see that all the empty spaces in the layout have been filled.

Image: Second Secon

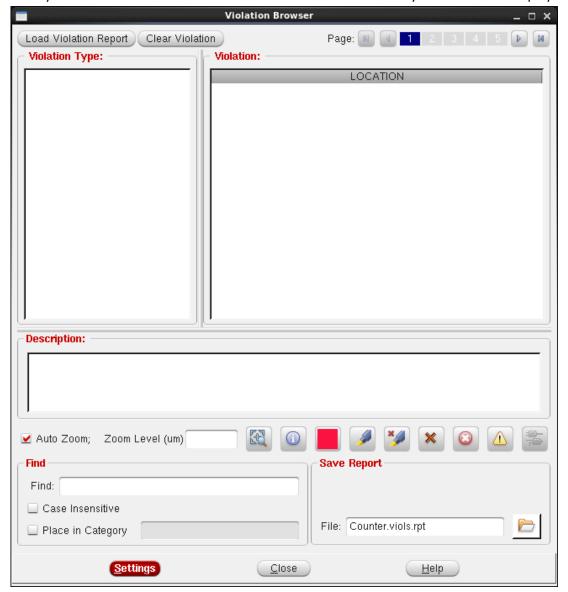
23. Now that the layout is complete, lets verify the layout. Let's verify the connectivity and geometry. Select Verify -> Verify Geometry and Verify -> Verify Connectivity. Use the default values for both cases. You will see the results in the terminal window. i.e.

```
VERIFY GEOMETRY ..... Cells
                                     : 0 Viols.
 VERIFY GEOMETRY ..... SameNet
                                     : 0 Viols.
 VERIFY GEOMETRY ..... Wiring
                                     : 0 Viols.
 VERIFY GEOMETRY ..... Antenna
                                     : 0 Viols.
 VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
 Cells
             : 0
 SameNet
             : 0
 Wiring
            : 0
 Antenna
            : 0
 Short : 0
```

```
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
********End: VERIFY GEOMETRY********
Begin Summary
Found no problems or warnings.
End Summary
```

******* End: VERIFY CONNECTIVITY *******

24. Once you have run both select **Tools->Violation Browser** and fix any errors that are displayed.



Hints:

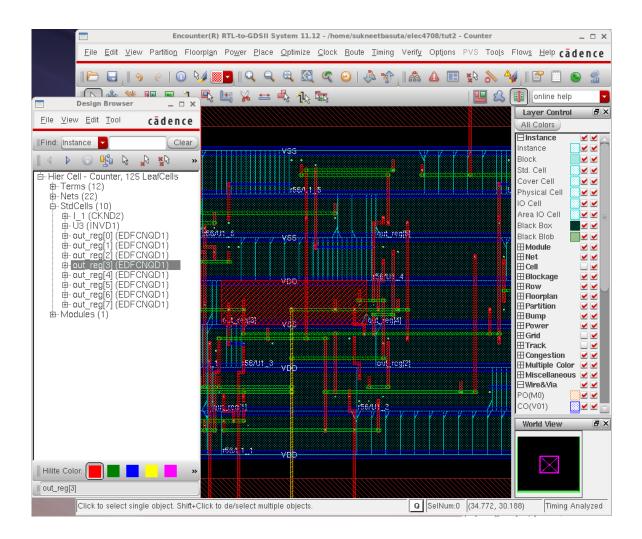
- Some routing errors are due to insufficient space. A solution is to make the chip area larger
- 25. Now that the layout is done, we can get a summary report. Select **File -> Report -> Summary** In the Summary Report window, you can select a text and/or HTML report

Summary Report _ 🗆 X
Report Format
🔾 Text Only 🛛 File: summaryReport.rpt 📄
O HTML Only
• HTML and Text
Output Directory: summaryReport 🖻
✓ Display HTML
<u>O</u> K <u>A</u> pply <u>C</u> ancel <u>H</u> elp

The HTML report will be located at something like summaryReport/Counter.main.htm in your lab2 directory. The Text report will be located at summaryReport/Counter.main.ascii.

۲		ncounter Report - Mozilla Fir	efox	_ = ×
File Edit View History	Bookmarks Tools Help 단			
	VI			
file:///home/suk	neetbasuta/elec4708/tut2/summaryReport/	'Counter.main.htm	☆ ✔ 😂 🛛 🕄 ✔ Google	🔜 🖖 🖀
###########	##################	#############	###################	2
# Generated by:	Cadence Encounter 11.12-	s136_1		
# OS:	Linux x86_64(Host ID loki)		
# Generated on:	Thu Nov 20 19:29:24 2014			
# Design: /TD>	Counter			
# Command:	summaryReport -outdir su	mmaryReport -brow	ser	
###########	###################	##############	##################	
Design Summ	arv Report			
besign ounn	ary Report			
General Design	Information			
Design Status		Routed	-1	
Design Name		Counter	-	
# Instances		125	-	
# Hard Macros		0	-	
# Std Cells		125	_	
# Pads		0	-	
# Net.		32	-	
# Special Net		2	-	
# IO Pins		12	-	
# 10 F IIIS # Pins		85	-	
# PG Pins		250	-	
Average Pins Per	Net(Signal)	2.656	-	
Average rins rei	iver(Signal)	2.050		
General Library	Information			
5			_	
# Routing Layers				
# Masterslice Lag	5		_	
# Pin Layers	4			
# Layers	22			
# Pins without Pl	nysical Port 0			
# Pins in Library	without Timing			

26. You can also use the design browser (located under the tools pull down menu) to locate the individual cells, module, nets, etc. To open the design browser, select **Tools-> Design Browser** The following picture shows the results browser and the selected module in red in the encounter window.



27. We have gone through a simplified design flow. There are many options that we haven't had a chance to explore. It might be a good idea to take a look at some of the available options. Like RC extraction or the various routing options.

Generally the last step in a design flow is to send a completed design to the fabrication facility. To do this the design is exported to a GDS2 file. To generate a GDS2 file we need a map file that relates layer names to numbers. Select **File -> Save -> GDS/OASIS**.

Name the output stream file anything you want (should be related to what the design is) with the gds2 extension. Make sure the map file is "streamOut.map" and the "Structure Name" is the name of your layout. click "OK".

	GDS/OASIS Export _ 🗆 X					
Output Form	at 🧕 GDSII/Stream 🔾 OASIS					
Output File	Output File count.gds2					
Map File	streamOut.map 🖻					
Library Nam	e DesignLib					
🕑 Structure I	Name Counter					
🔲 Attach Ins	stance Name to Attribute Number					
🔲 Attach Ne	t Name to Attribute Number					
🔲 Merge File	es 📄 📄 Uniquify Cell Names					
📃 Stripes	1					
🔲 Write Die .	Area as Boundary					
🔲 Write abstr	Write abstract information for LEF Macros					
Units 2000 🕨						
Mode ALI						
<u>о</u> к	<u>Apply</u> <u>Cancel</u> <u>H</u> elp					

28. Congratulations, you have now completed the tutorial for a simplified Encounter design flow.

Timing Report

- In the terminal window you opened encounter in, type report_timing
- The timing report will be printed in the console. The Arrival time is the worst case delay in ns. In the example below, the longest path delay is 0.826 ns.

i.e.	-	5	
-			
Analysis View: worst_view			
Other End Arrival Time	0.03	2	
- Setup	0.11	3	
+ Phase Shift 1	10.00	0	
= Required Time	9.91	9	
- Arrival Time	0.82	6	
= Slack Time	9.09	3	
Clock Rise Edge		0.000	
+ Clock Network Latency (Pr	rop)	0.032	
= Beginpoint Arrival Time		0.032	
+			+
Instance Arc		Cell	Delay Arrival Required
I İ			Time Time

++++++		++	+	
out_reg[0] CP ^			0.032	9.124
out_reg[0] CP ^ -> Q v	EDFCNQD1	0.145	0.177	9.270
r56/U1_0 A v -> CO v	FA1D1	0.141	0.318	9.411
r56/U1_1 CI v -> CO v	FA1D1	0.072	0.390	9.483
r56/U1_2 CI v -> CO v	FA1D1	0.071	0.461	9.554
r56/U1_3 CI v -> CO v	FA1D1	0.070	0.531	9.624
r56/U1_4 CI v -> CO v	FA1D1	0.071	0.602	9.695
r56/U1_5 CI v -> CO v	FA1D1	0.070	0.672	9.764
r56/U1_6 CI v -> CO v	FA1D1	0.068	0.740	9.833
r56/U1_7 CI v -> S ^	FA1D1	0.086	0.826	9.919
out_reg[7] D ^	EDFCNQD1	0.000	0.826	9.919
+				+

 If you wanted to the delays of other paths, you can do report_timing -max_paths 5 where the number of max_paths prints n paths delays in descending order (n is 5 in the above command).

Power Report

• Select **Power -> Power Analysis -> Setup** to setup the power analysis. Select the analysis view you created in Step 7. User the max Corner.

Set Power Analysis Mode	×
Basic Advanced	1
Analysis Method: Image: Static Image: Dynamic Dynamic Power Method: Image: Vectorless Image: Vectorbased Image: Disable Static Analysis Image: Disable Static Analysis Image: Disable Static Analysis	
Analysis View worst View Corner: max Switched-off or Power-up Nets:	
 ✓ Create Power Binary Database ✓ Write Current Files 	
PowerGrid Libraries:	P
<u>O</u> K <u>Apply</u> <u>S</u> ave <u>L</u> oad <u>C</u> ancel) <u>H</u> elp

• Select **Power -> Power Analysis -> Run**. The Run Power Analysis window will popup. Here you can specify the input activity and Clock Frequency (Dominant Frequency).

		Run Power An	alysis		_ 0
Basic Activity Po	wer Power-Up	Advanced			
Input Activity: 0.2		Dominant Frequency: 10	0	(MHz)	
Flop Activity:		Clock Gate Activity:			
Activity File: 💿 🗸	/CD 🔾 FSDB 🦳			🖻 (Add) Remove Vector Profil	er
Scope:	Start:	(ns) Stop:	(ns) Block		
Туре	File	Scope Star	Stop	Block	=
Results Directory:				<u>P</u>	2
<u></u> K	Apply	Save	Load	Cancel Help	

• Hit OK and the power consumption will be displayed in the terminal. Note that the power consumption is displayed in mW, and a V_{DD} of 0.9V is used by default.

.

ne. Total	Power			
Total	0	0.0123 0.001449	78.72% 9.267%	
	Leakage Power: Power: 0.0156		12.02%	