Lab 1: Schematic and Layout of a NAND gate

In lab 1, our objective is to:

- Get familiar with the Cadence Virtuoso environment.
- Draw a schematic of a simple NAND gate and simulate it.
- Draw layout of a NAND gate using cell library, then run a design rule check (DRC), extract, run a layout versus schematic (LVS) and simulate the extracted circuit.
- Compare the schematic and extracted simulations.

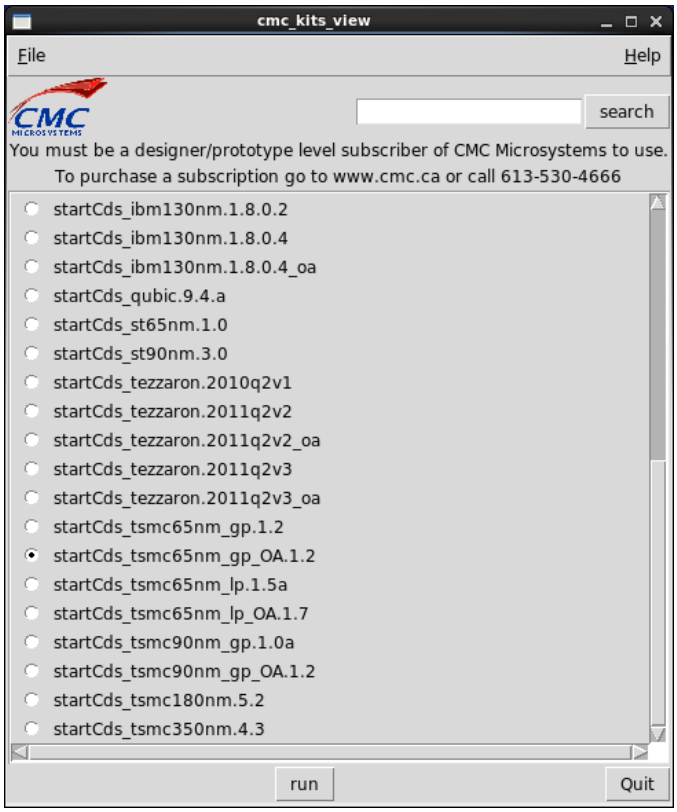
In this lab procedure, detailed procedures and snapshots are given for the sake of understanding. You are supposed to understand the procedures, so that you can design your own circuit later. The other lab procedures will not be as elaborate except where necessary. Please refer to this lab procedure in future labs for reference.

Login procedure:

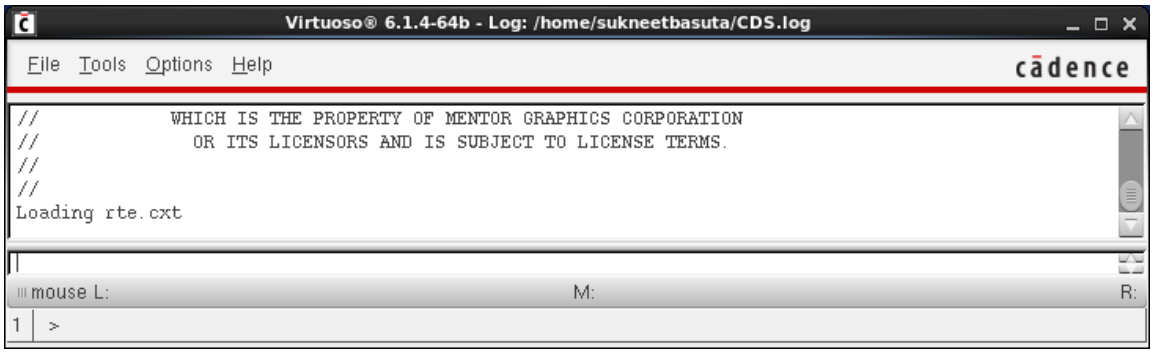
After logging in to the computer in the lab using your existing DoE accounts, double click on the "**Unix Systems**" icon to start the remote login server on the Unix machine. Choose one of the computers from the list and click "**Connect**". Ask the TA(s) for help if you have trouble. When you are prompted to enter your username and password, ask the TA(s) for your username and initial password. Make sure you **change your password** as soon as you log in for the first time and **remember** it for the rest of the labs. *The TA(s) might not be able to help you if you forget your password.*

PART A: Procedure

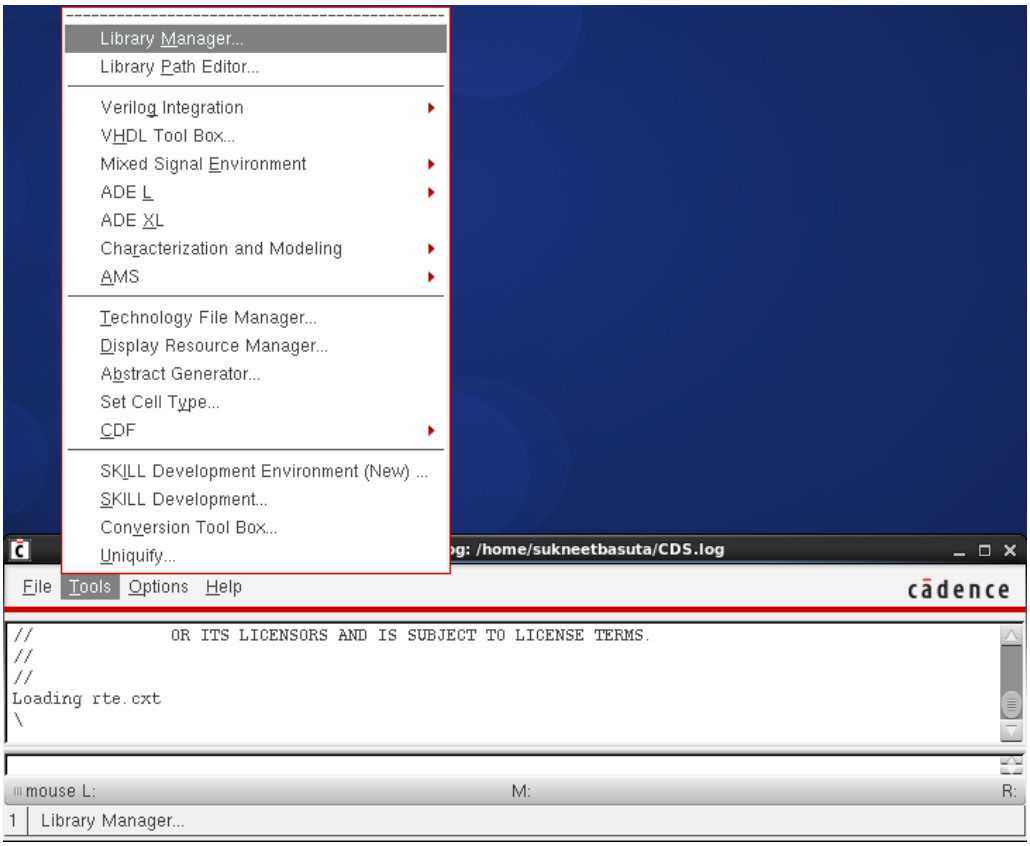
1. Open a terminal and create a folder in your home directory for Lab 1 "**elec4708/lab1**"
   ```
   > mkdir elec4708
   > cd elec4708
   > mkdir lab1
   > cd lab1
   ```
2. Start Cadence in the directory your just created. A window allowing you select the technology kit should popup. Select the TSMC 65nm GP (general purpose) OA technology kit. (Kits ending in OA will open in Cadence 6)
   ```
   > startCds
   ```



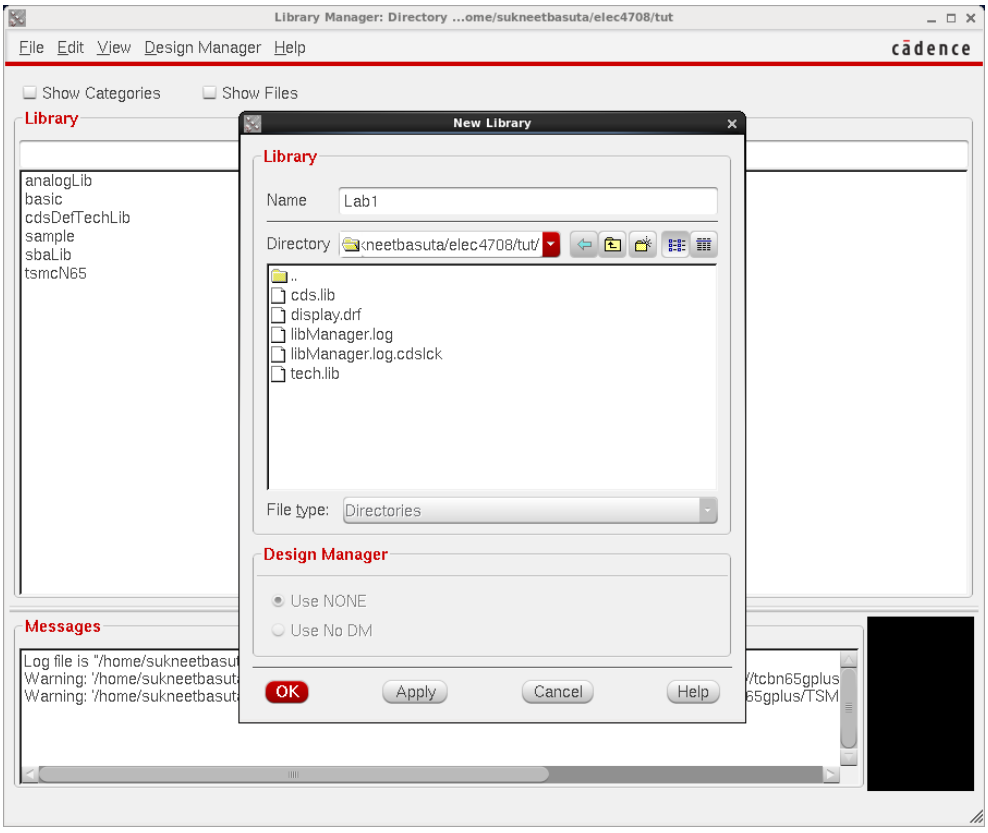
3. Close the “What’s New” window if it appears. The Virtuoso console should still be open.



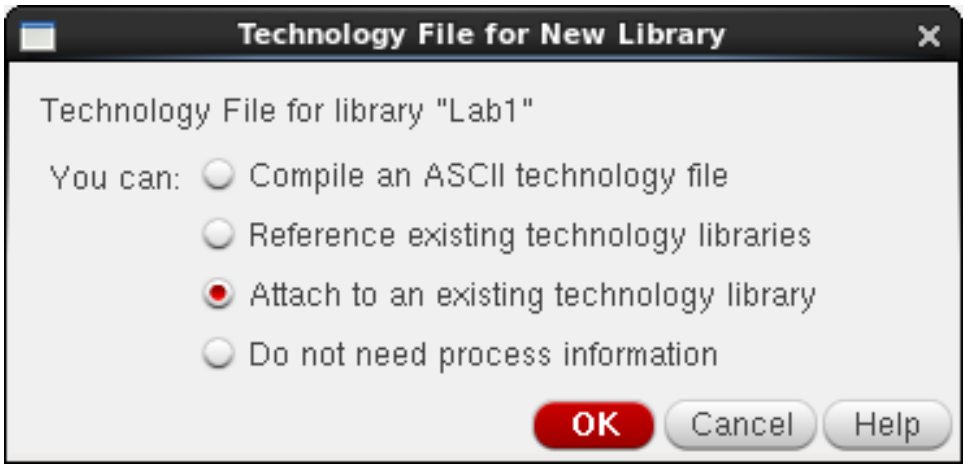
4. The next thing we will do is make a library to hold all your work for lab1. Click on **Tools -> Library Manager** (or simply press **F6**). Library manager window should pop up.



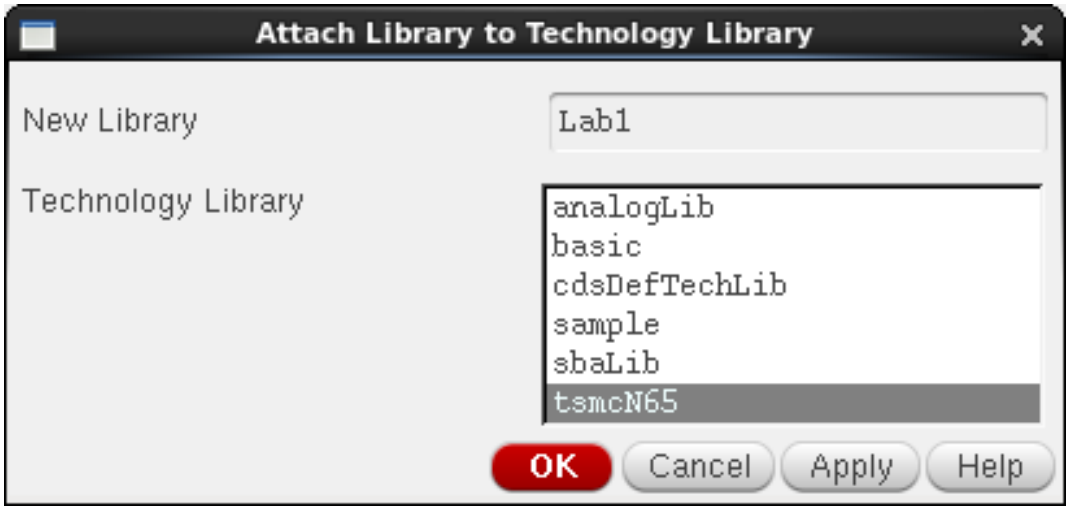
5. Click **File -> New -> Library**. Type “lab1” in Name field. Click OK.



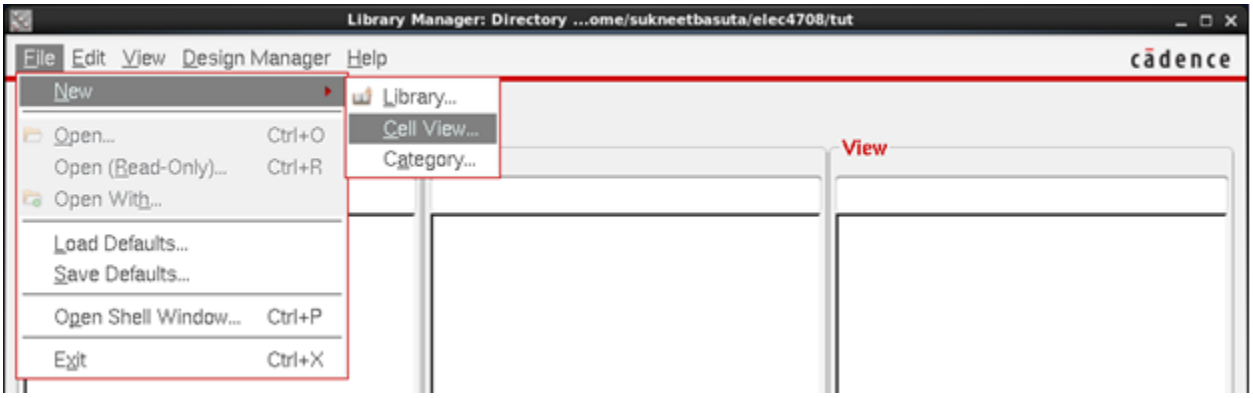
6. Select "**Attach to an existing techfile**" and Click OK.

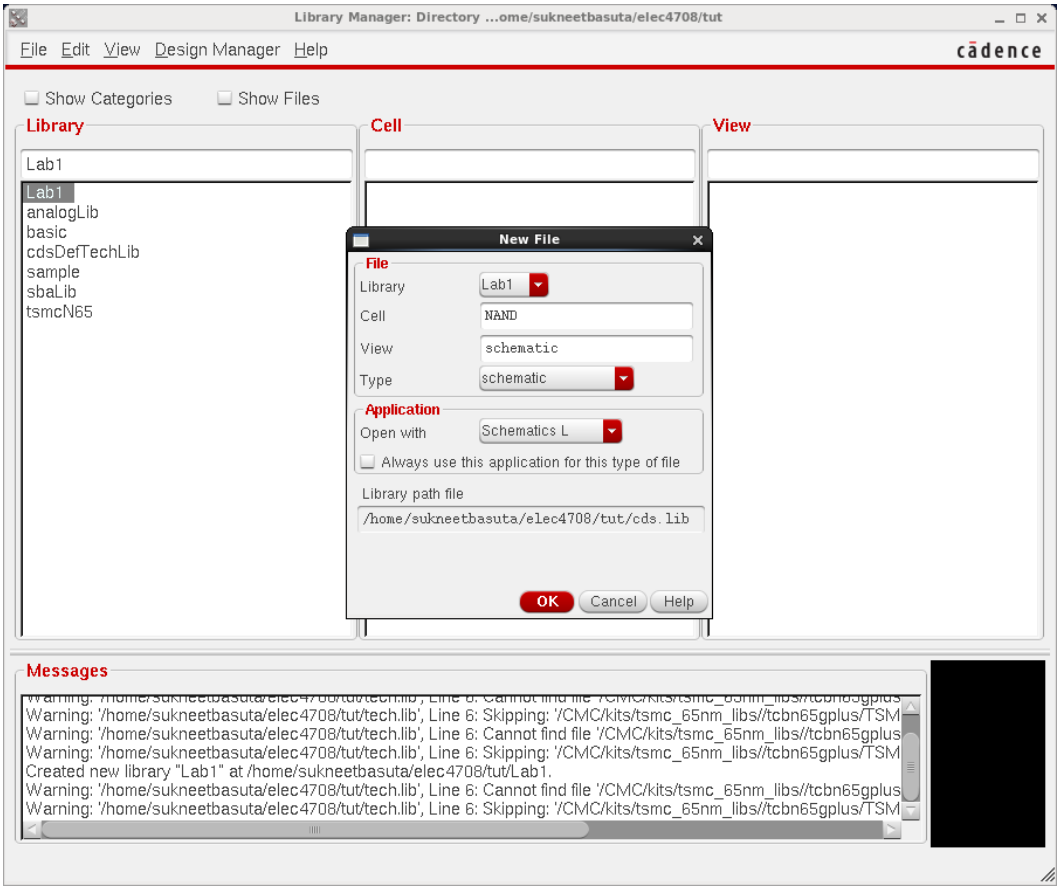


7. Select "**tsmcN65**" from the Technology Library list. Click OK.

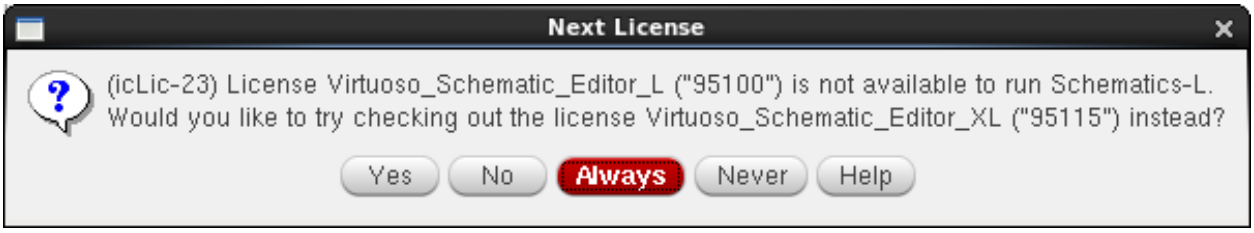


8. Highlight the new library you have just created, i.e. "lab1", and **click File -> New -> Cell View**. Type "**NAND**" in Cell Name. Keep the default values in other fields as shown. Click OK.

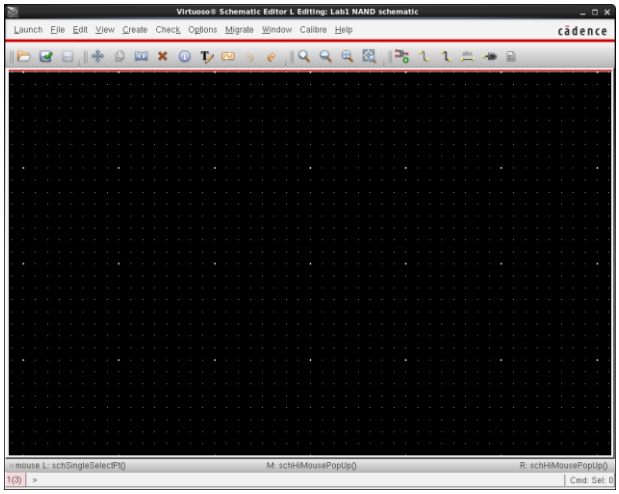




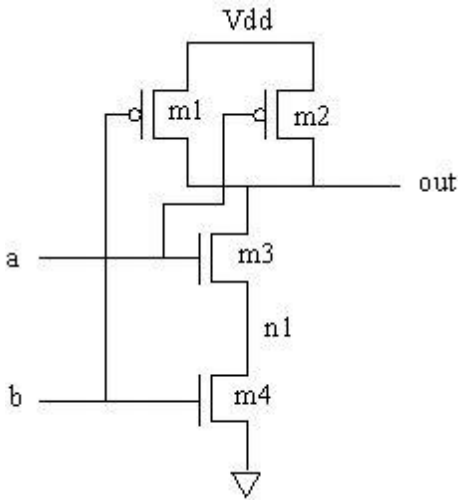
9. If a License error pops up like the one below, hit “Always”.



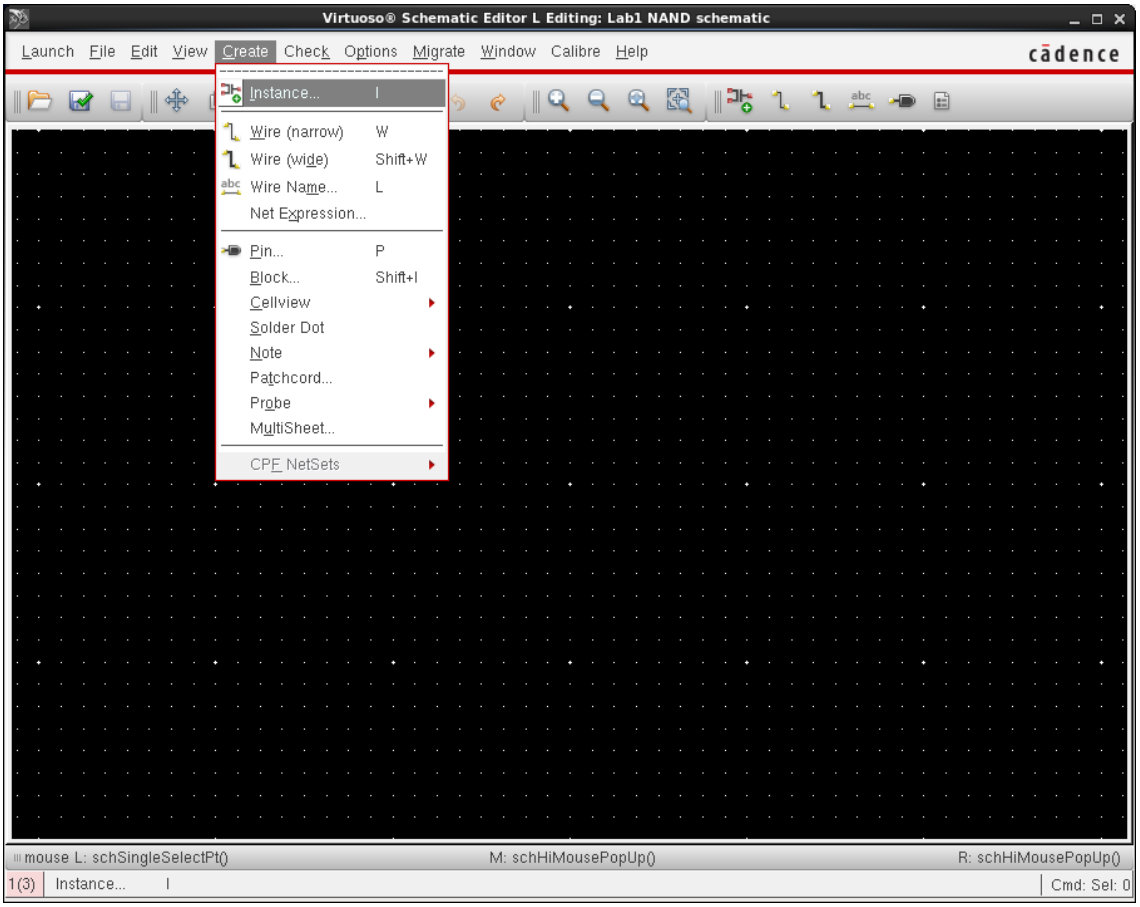
A blank Virtuoso Schematic Editing window will open. Move your cursor through the icons on the top toolbar and pop-up descriptions for each will show up.



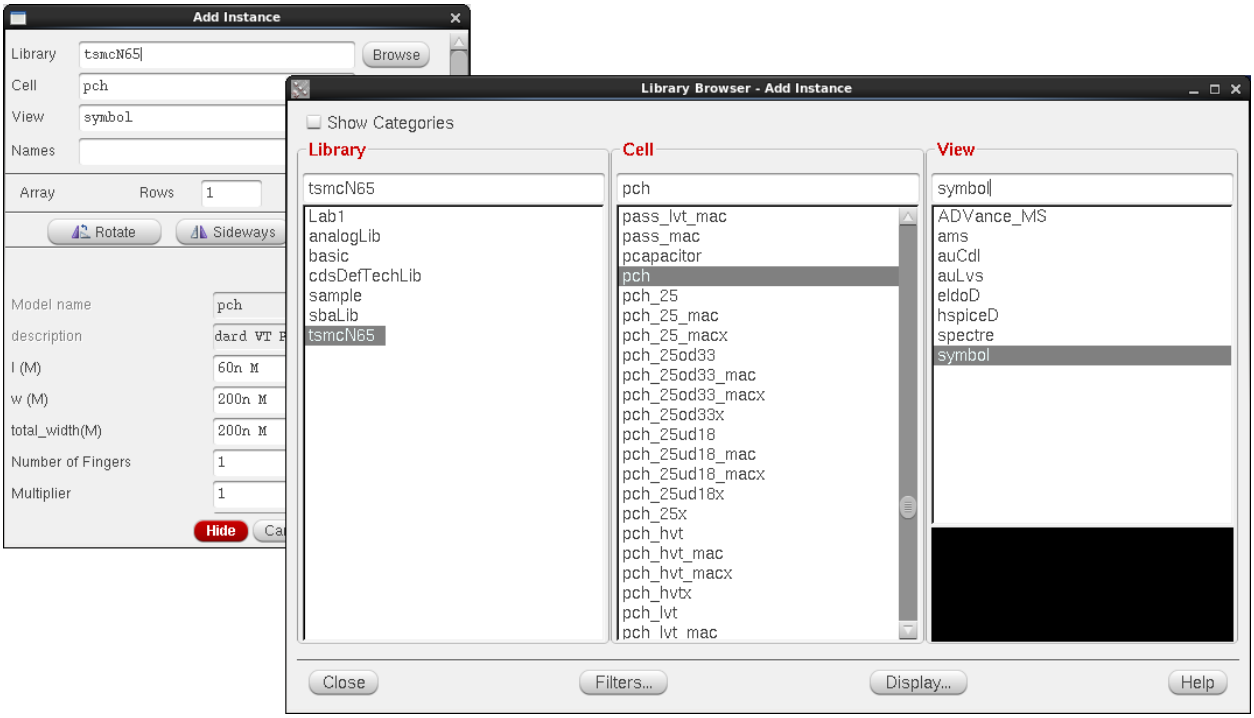
10. The next thing we will do is draw the NAND gate using pfets and nfets. We will also add 2 input pins, 1 output pin, 1 VDD pin and 1 GND pin. A circuit diagram of NAND gate is given here.



11. To add an instance in your schematic, you can click on the Add Instance icon  on the top toolbar, or click on **Create -> Instance**, or simply type "**i**" from the keyboard. The Add Instance dialog box will show up.

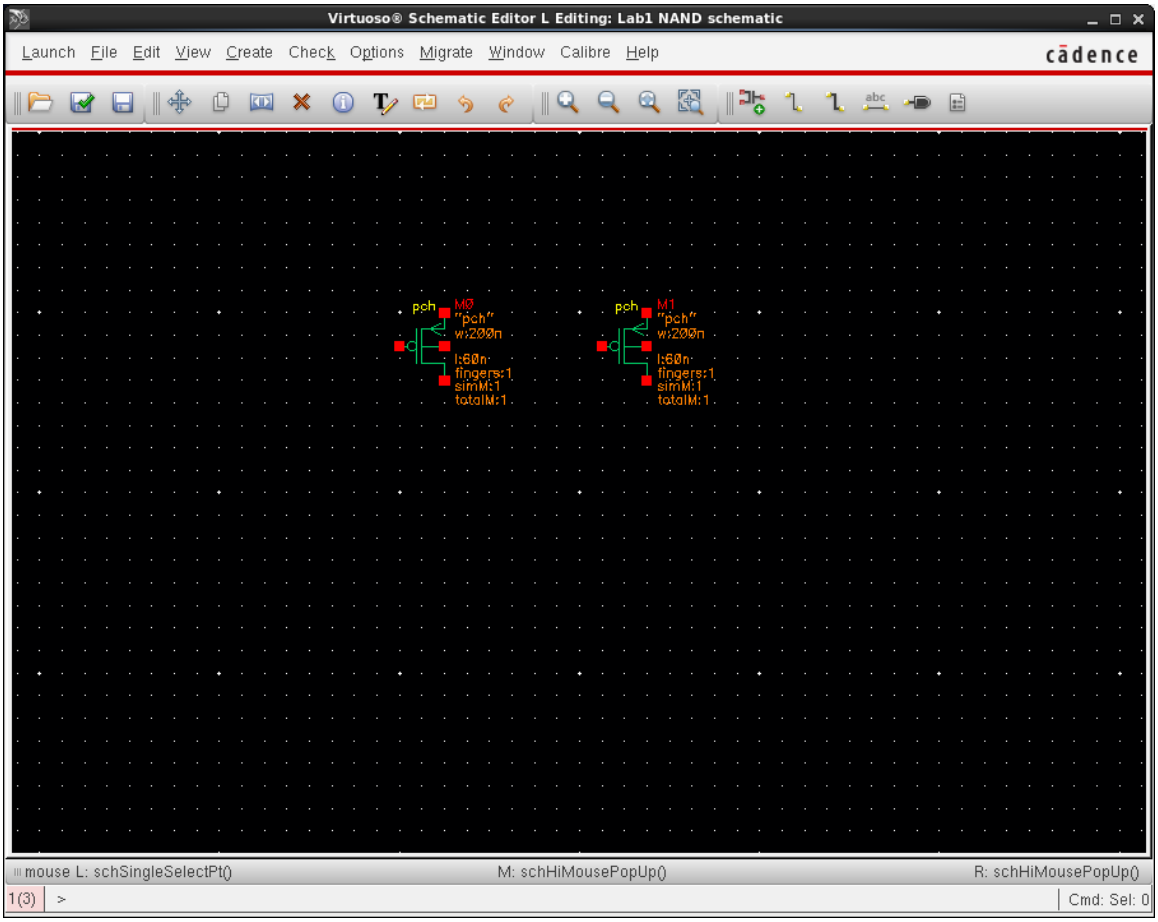


12. Click Browse beside Library. Library Manager will pop up.

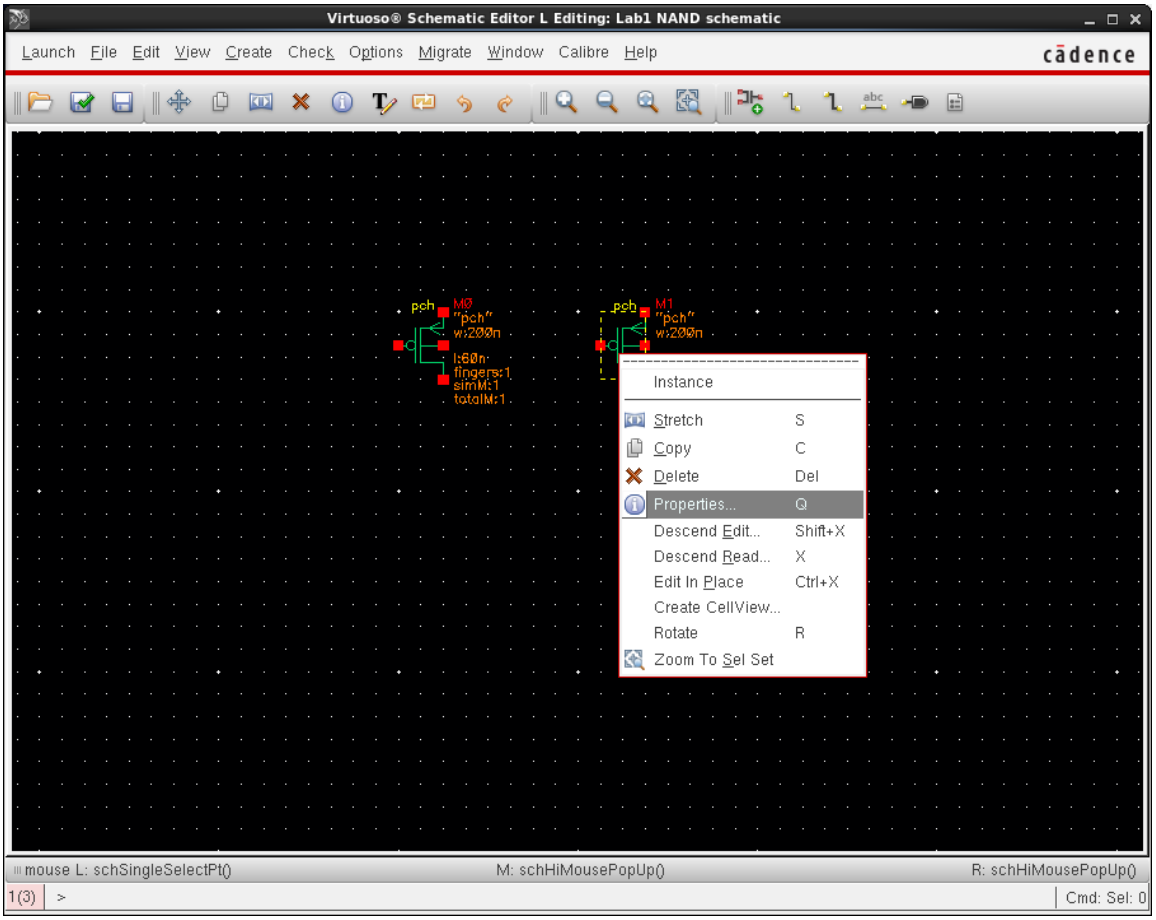


13. In Library, select “**tsmcN65**”, in cell select “**pch**” (for a pfet device), in view select “**symbol**”. Then click Close.

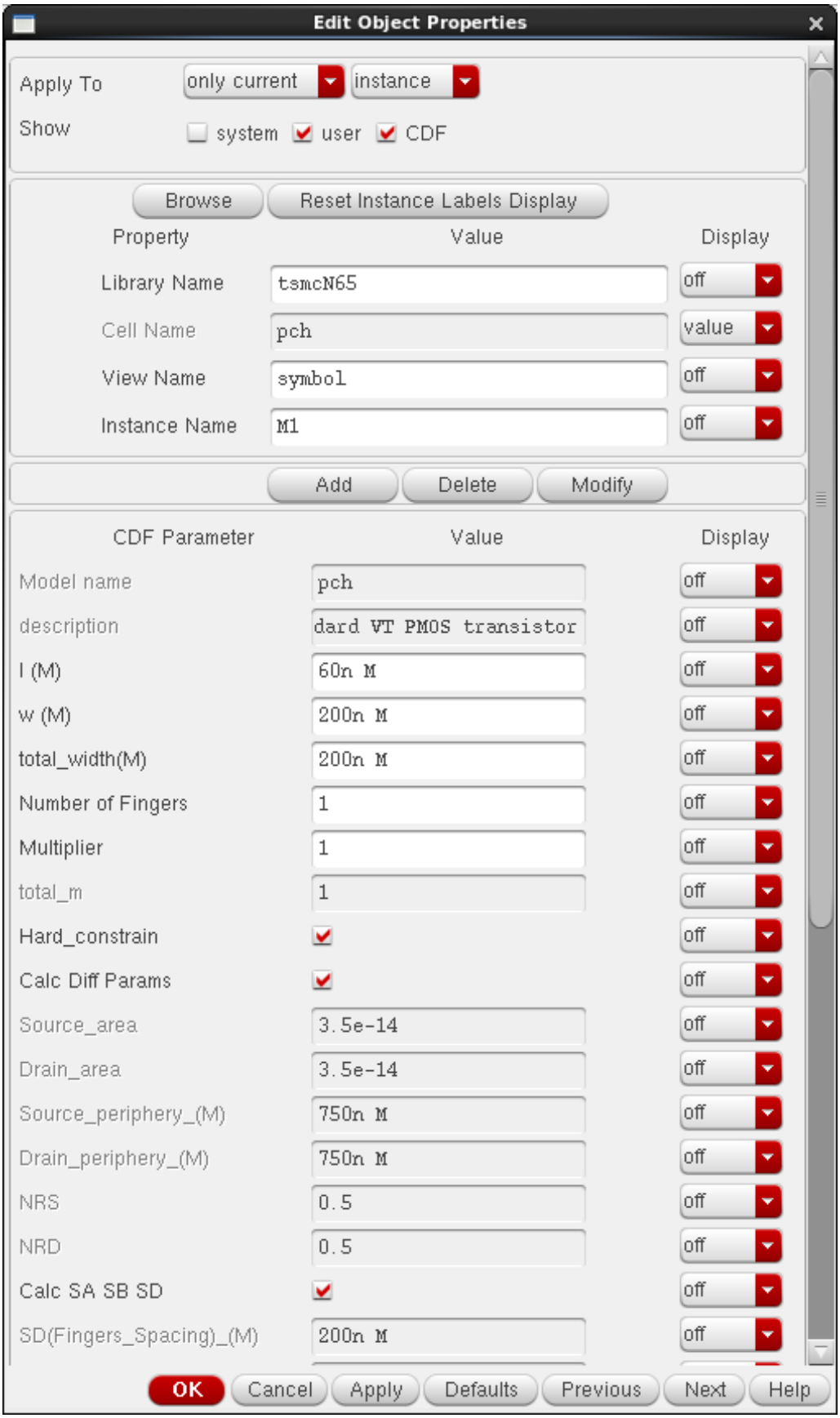
14. Close the Library Browser and, optionally, Hide the Add Instance window. Place the instance in your design. You can place multiple instances of same item, can rotate the instance by typing ‘**r**’ on your keyboard, or mirror the instance by hitting “**Shift+r**”. When you are done with placing all the instances of that item, **press Esc** to leave “Add Instance” mode.



15. You can access the object property window by right-clicking on an instance and selecting properties. Alternatively, you can select an instance and press "**q**".

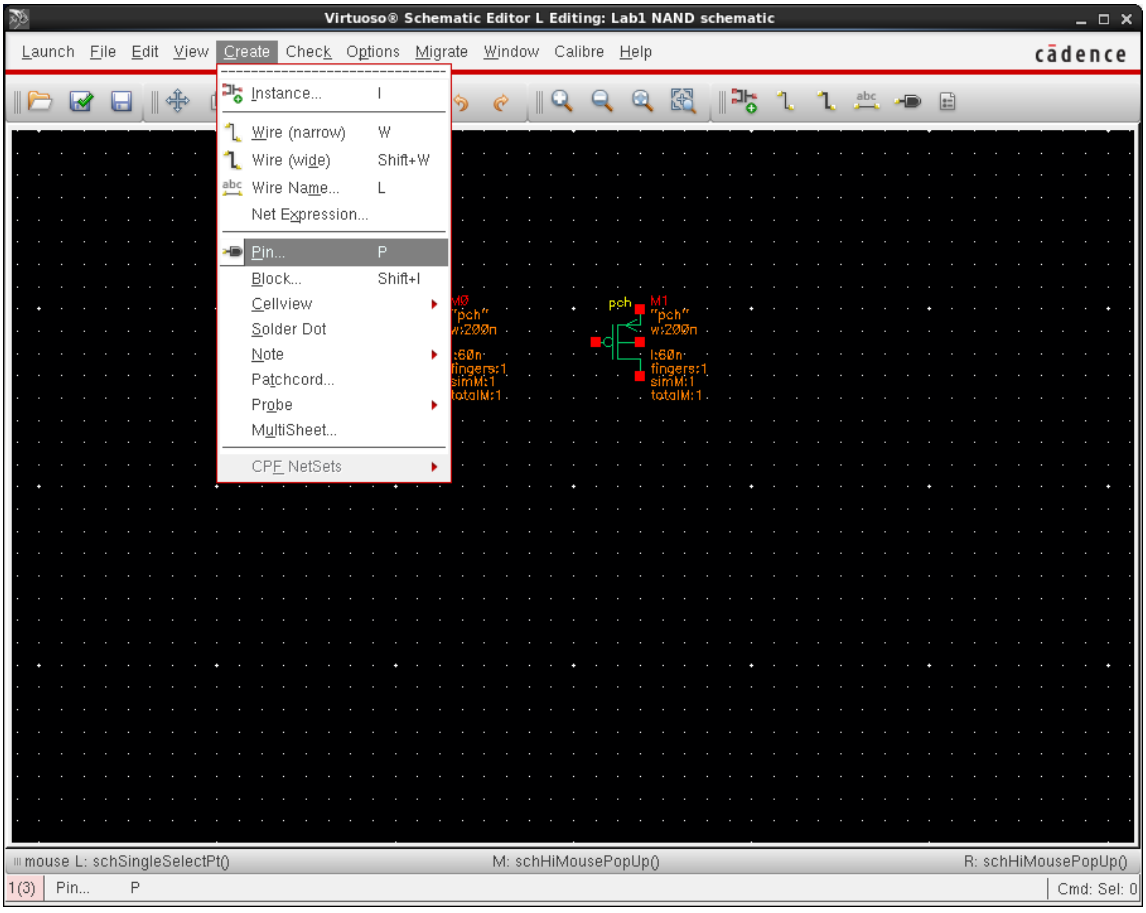


16. The Edit Object Properties window will pop up and will show properties of that instance. You can change length or width if required. For now, we will use default widths for pfets and nfets. However, you can change widths later to enhance performance. Note that the default length value is set to the minimum allowed by the technology, but this is not the case for the default width value. **NOTE: It is okay if the width rounds to the nearest multiple of 5.** Due to process variations, there is a limitation on accuracy.

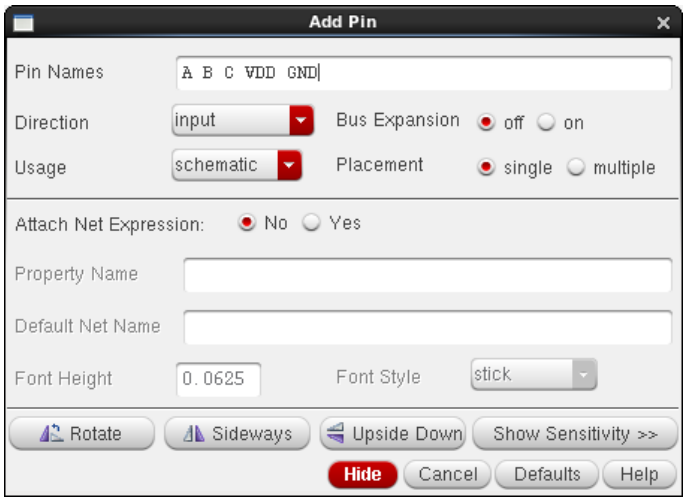

Edit Object Properties
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
tsmcN65
off
Cell Name
pch
value
View Name
symbol
off
Instance Name
M1
off
Add
Delete
Modify
CDF Parameter
Value
Display
Model name
pch
off
description
dard VT PMOS transistor
off
l (M)
60n M
off
w (M)
200n M
off
total_width(M)
200n M
off
Number of Fingers
1
off
Multiplier
1
off
total_m
1
off
Hard_constrain
off
Calc Diff Params
off
Source_area
3.5e-14
off
Drain_area
3.5e-14
off
Source_periphery_(M)
750n M
off
Drain_periphery_(M)
750n M
off
NRS
0.5
off
NRD
0.5
off
Calc SA SB SD
off
SD(Fingers_Spacing)_(M)
200n M
off
OK
Cancel
Apply
Defaults
Previous
Next
Help

17. Repeat steps 11. to 14. for the nfets ("**nch**" from the same library) and place them in your design.

18. To input and output signals, you need to add pins. To add pins, click on the Create Pin  button on the top toolbar, or click **Create -> Pin**, or simply type "**p**" from the keyboard. Add Pin dialog box will open.

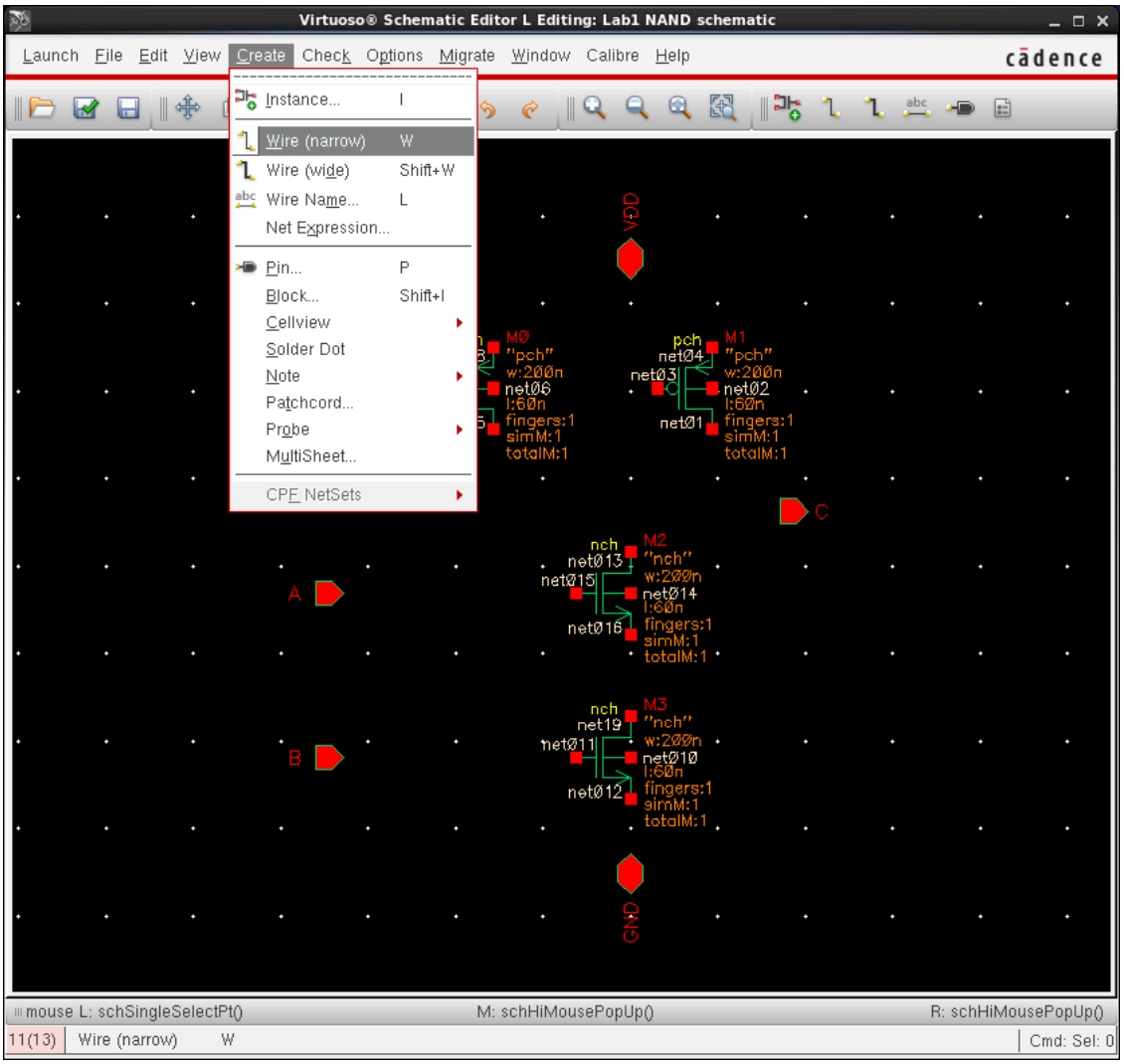


19. Type the names of the pins you want to add in sequence, leaving a blank space in between. DO NOT click Hide button. You will need to change Direction property for some of the pins.



20. Click on the schematic where you want to place pin A. For pin A and B direction should be input, for pin C direction should be output, for pin VDD and GND direction should be inputOutput. Now click “Cancel” in the Add Pin dialog box.

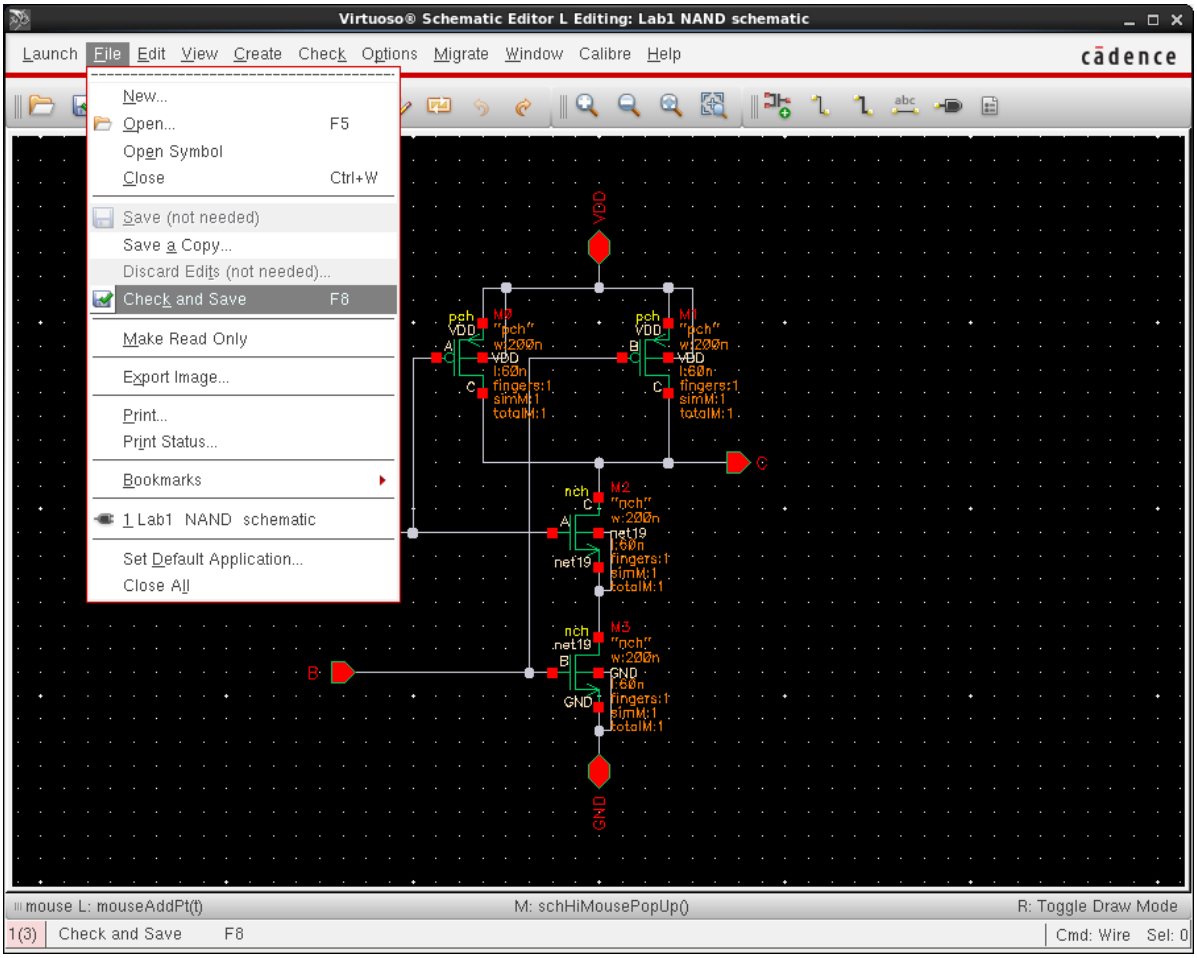
21. To add wires, you can click on Wire (narrow) icon  on the top toolbar, or click Create -> Wire (narrow), or simply type “w” from the keyboard. The Add Wire dialog box will open.



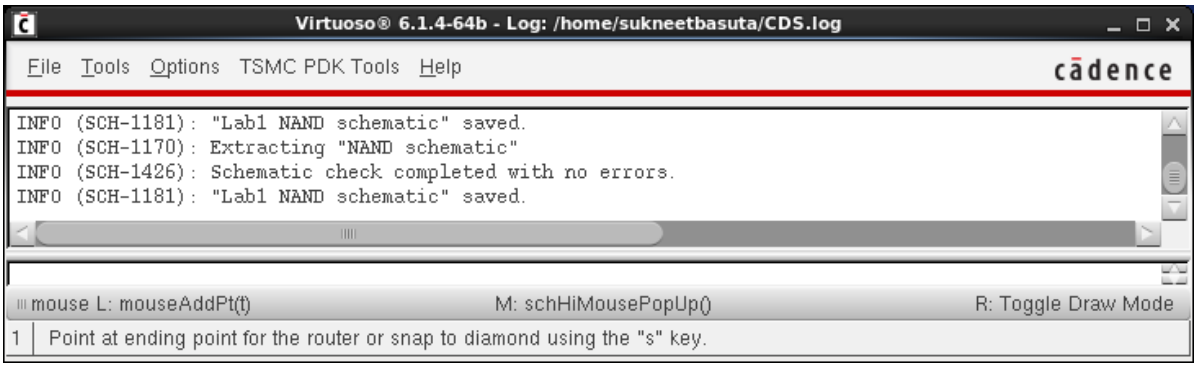
22. Connect the pins with FETs properly to form a NAND gate. Notice that you have to connect the substrate of pfets and nfets properly.

23. Now that the schematic is completed, we must save it and check for any errors or warnings.

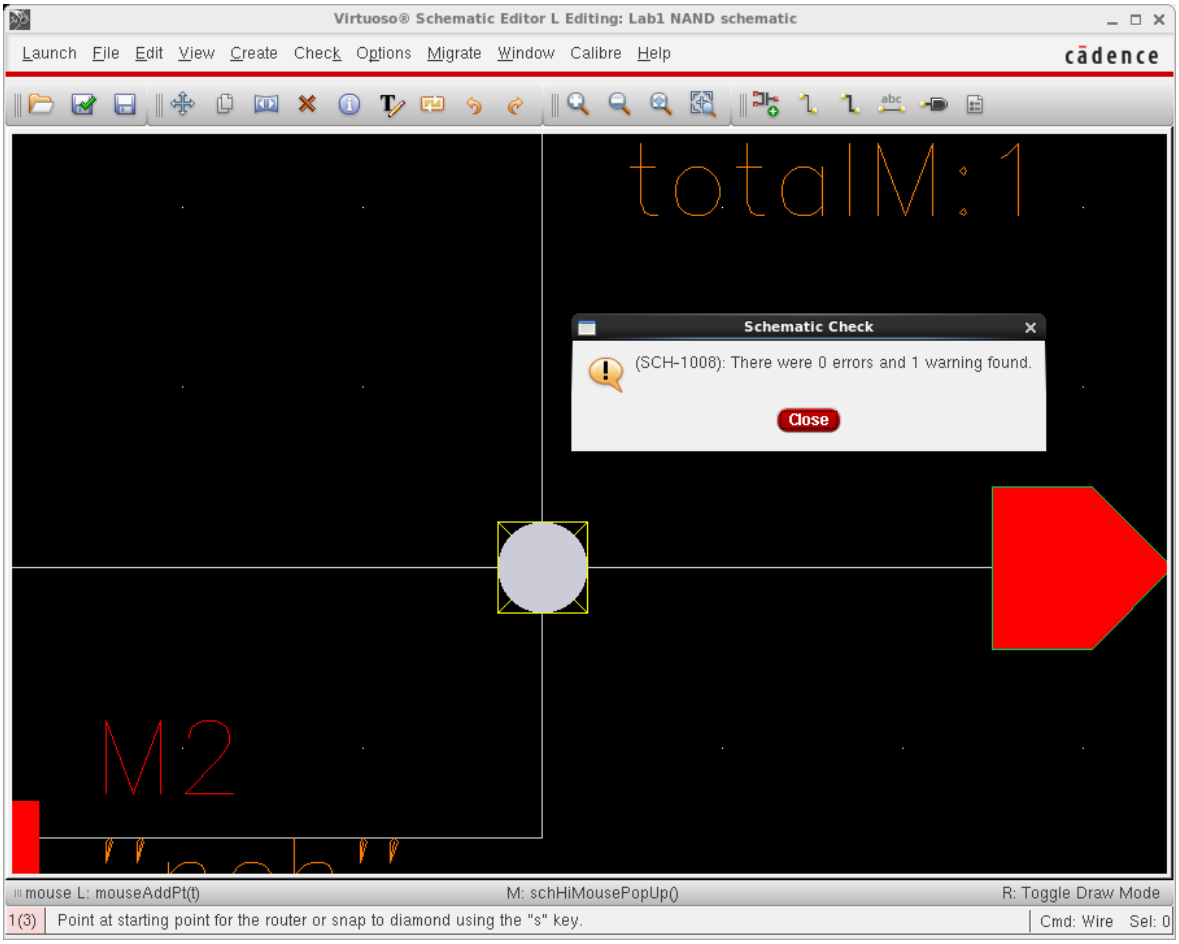
    To do both operations at once, click the on “**Check and Save**” icon  on the top toolbar, or click **File -> Check and Save**, or simply hit **F8** on the keyboard.



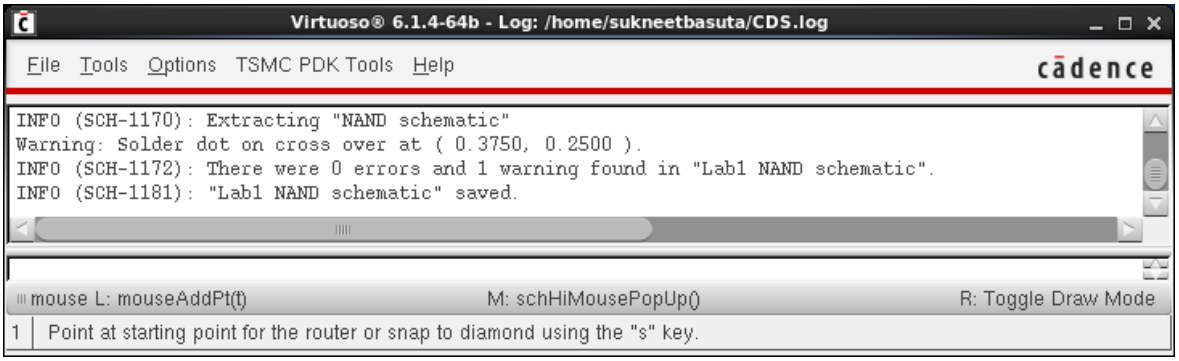
24. If there are no errors, nothing will popup and the Virtuoso console will state the save completed with no errors.



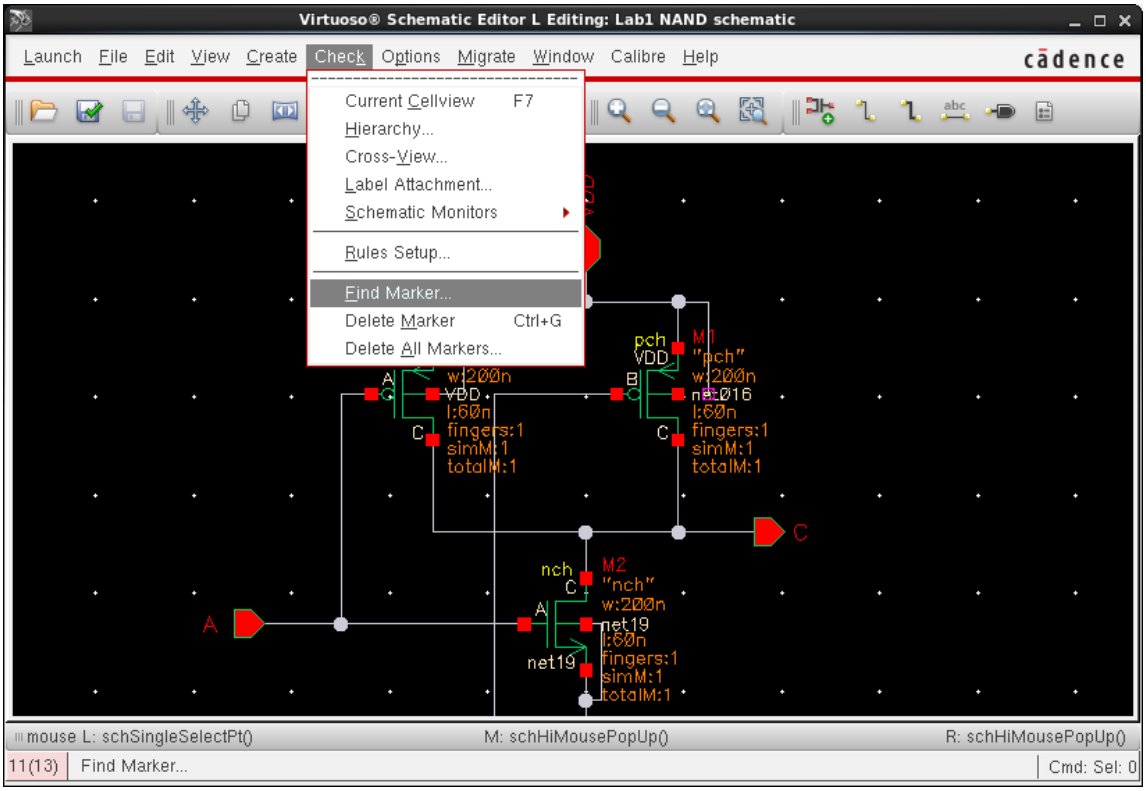
If there are any errors, a window will popup stating how many errors and warnings are found. Any problems will surrounded by a flashing yellow box in the schematic view.

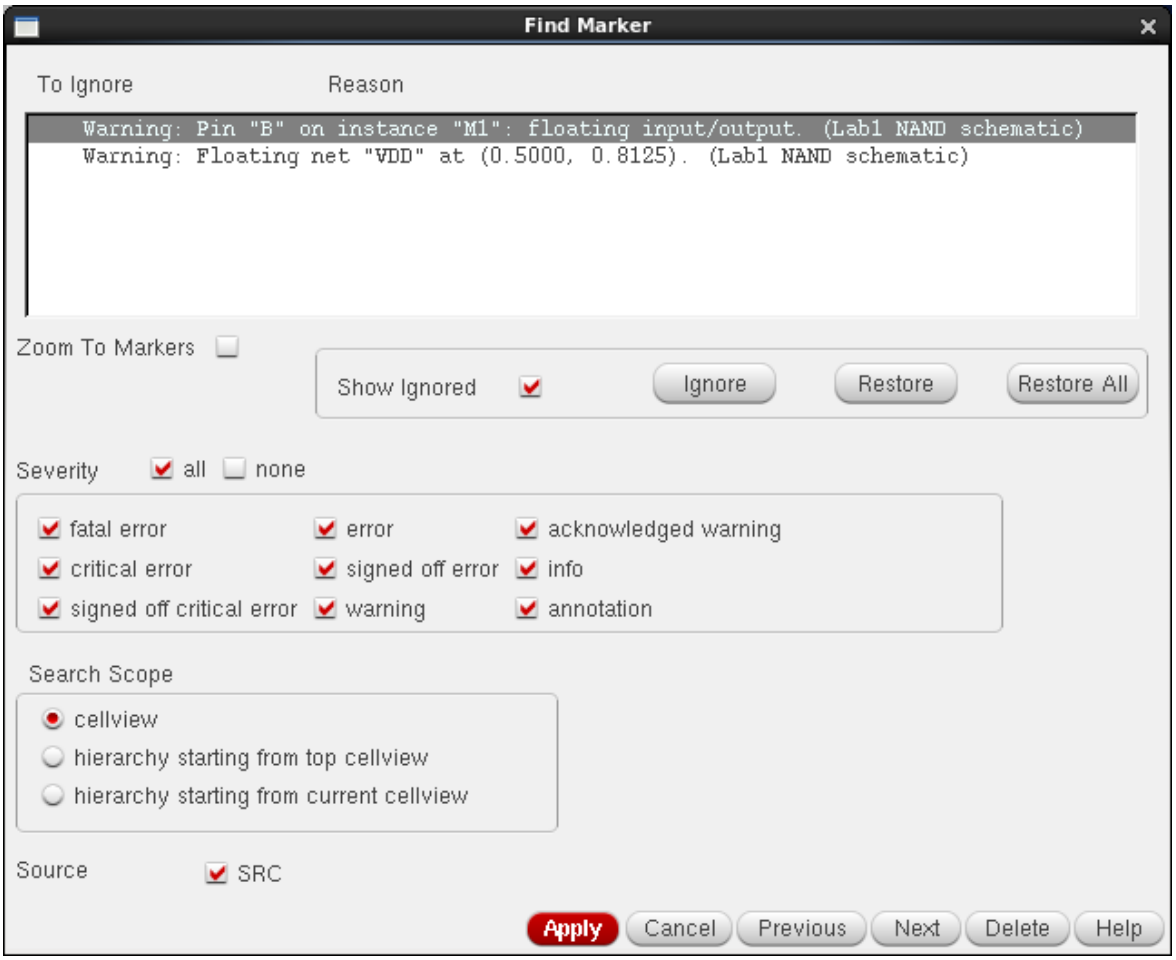


If you cannot see the problems or want more details, look at the Virtuoso console. It will explicitly state what the issue is and where it occurs.



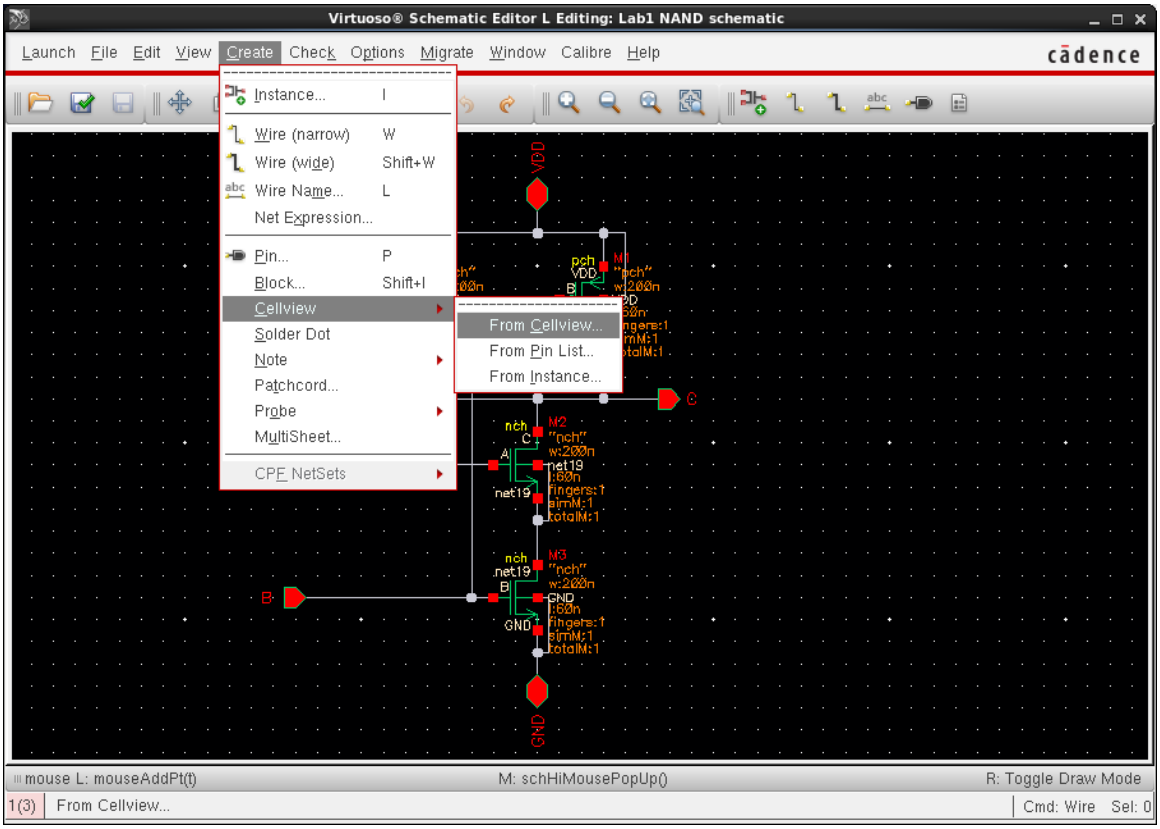
Alternatively, an easier way to discover problems is to use Find Marker. In Find Marker, you can click on the details of each warning and/or error to highlight it in the schematic. If the “Zoom to Markers” option is checked, it will also zoom in on the error when each warning and/or error is clicked. The Find Marker screen is opened by going to Check->Find Marker…


Virtuoso® Schematic Editor L Editing: Lab1 NAND schematic
Launch File Edit View Create Check Options Migrate Window Calibre Help
cadence
Current Cellview F7
Hierarchy...
Cross-View...
Label Attachment...
Schematic Monitors
Rules Setup...
Find Marker...
Delete Marker Ctrl+G
Delete All Markers...
pch
VDD
M1
"pch"
w:200n
l:60n
fingers:1
simM:1
totalM:1
nch
M2
"nch"
w:200n
net19
A
B
C
mouse L: schSingleSelectPt()
M: schHiMousePopUp()
R: schHiMousePopUp()
11(13)
Find Marker...
Cmd: Sel: 0

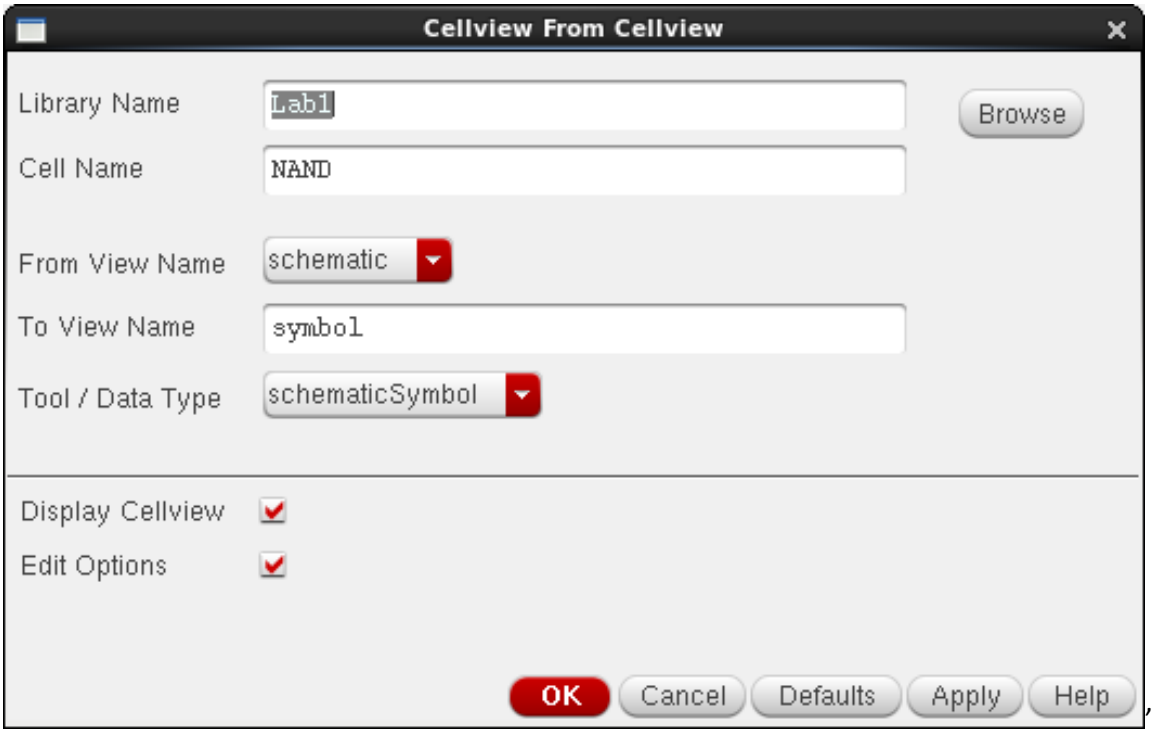


Note that Virtuoso will produce a warning if a junction has more than 3 wires connected. To avoid this, you can reroute one wire to form 2 junctions instead of 1. Get rid of all errors and warnings. If you need help, ask the TA(s).

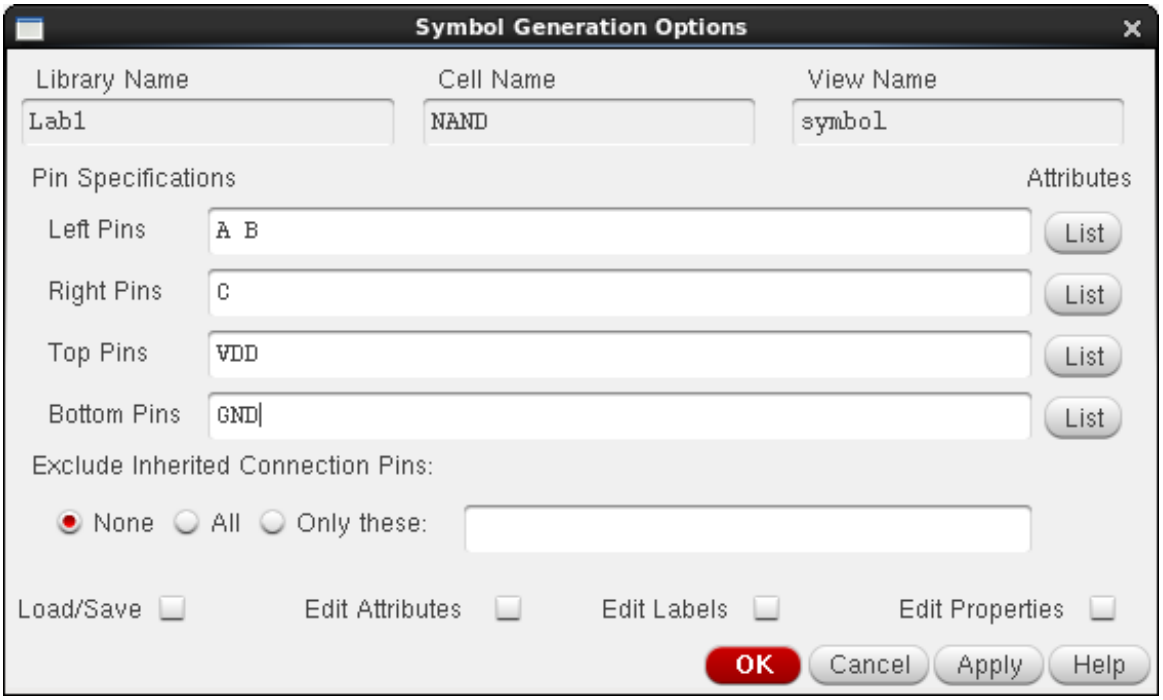
25. To make schematics clearer and cleaner, we will create a symbol for the NAND gate.
    To do this Click **Create -> Cellview -> From Cellview**. The “Cellview From Cellview” dialog box will open.



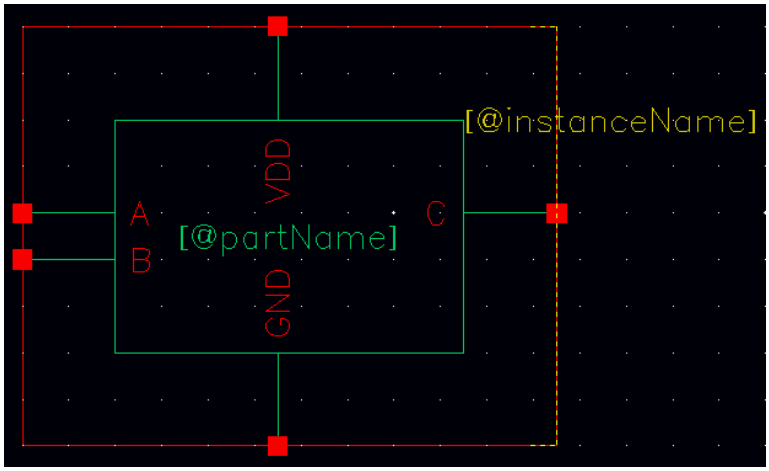
26. Keep the default values as shown and click OK.



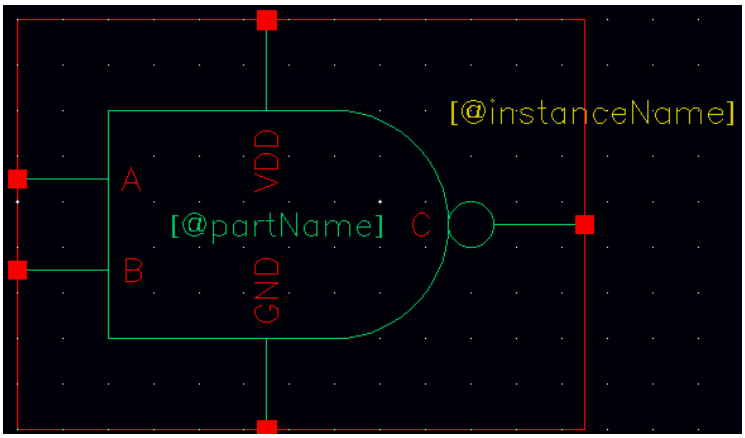
27. In the Symbol Generation Options, you can specify the location of each pin in the generated symbol. It will try to guess the best location for each pin based on the pin Direction.



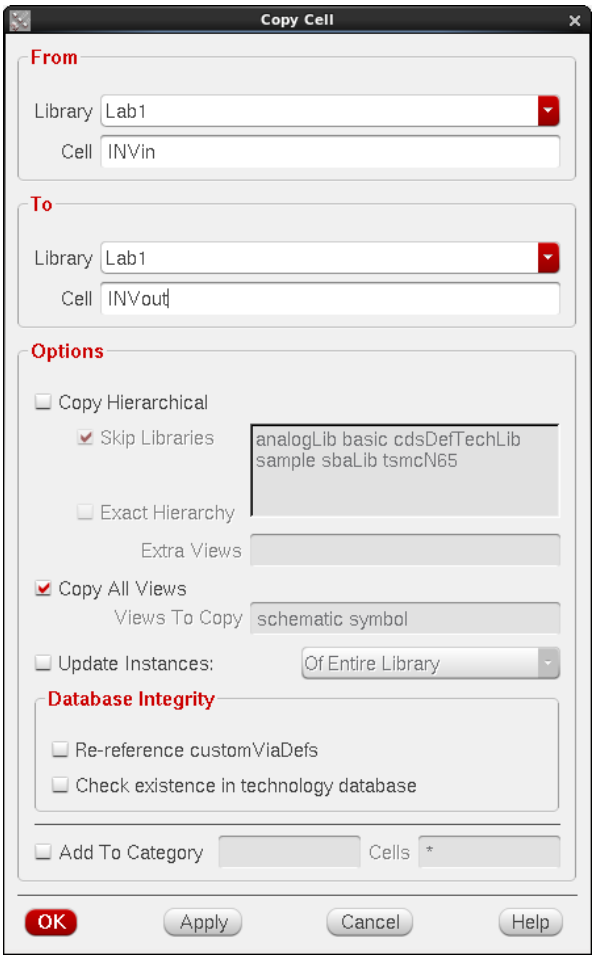
28. The Virtuoso Symbol Editing window will open. You can keep the default rectangular shape or change it to your own as you like. You can click and drag on an edge to increase or decrease the size of a shape and you can rotate shapes with the ‘r’ key on your keyboard. To change shape, select and delete rectangular box, click on Line icon in the left side toolbox, select shape and line width as necessary and draw a new shape. You can also move the pins around if you like. This step is optional.



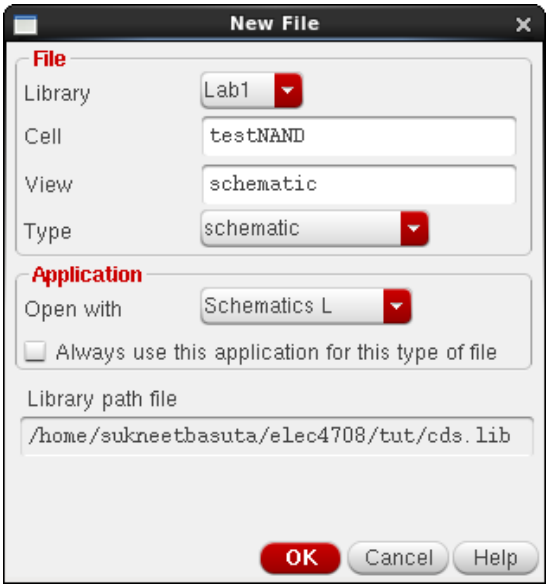
(optional)



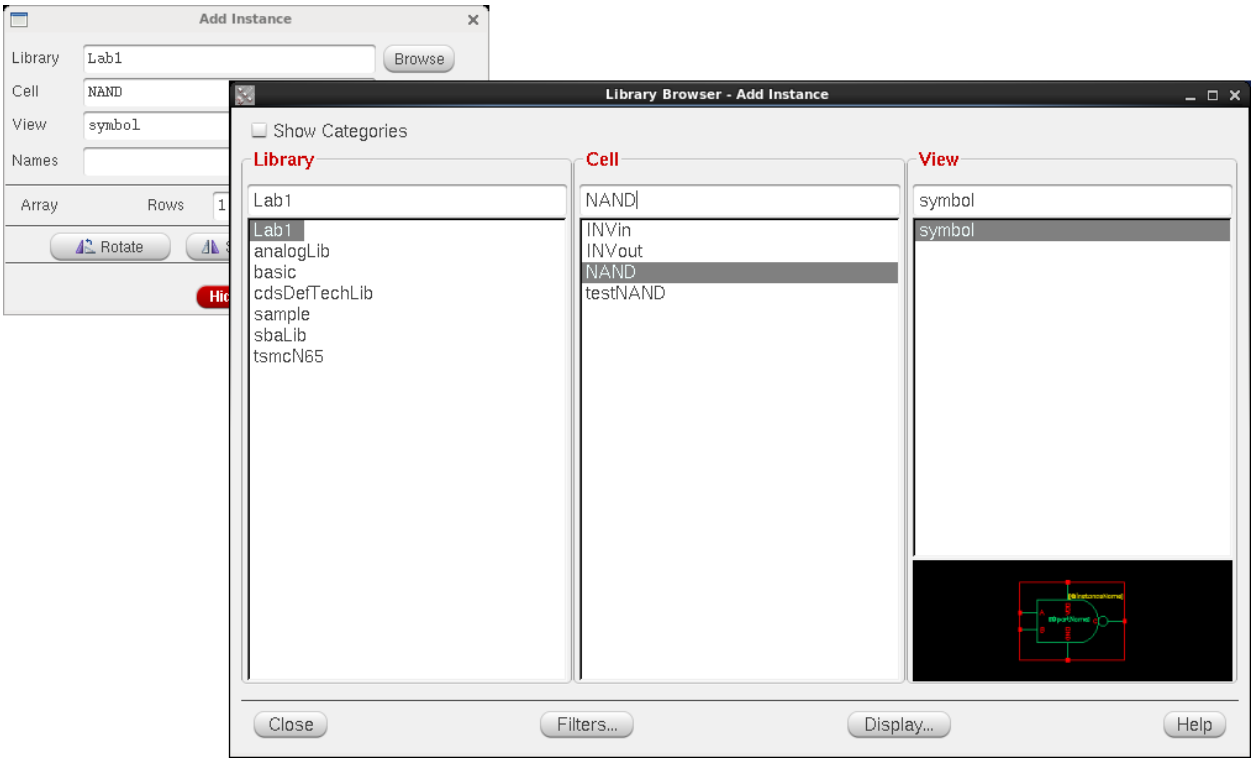
29. Save and close the symbol window and schematic window. You will also need to create 2 **inverter schematics and symbols** using the same procedure (step 8 to 27). Name your inverter as **INVin**. To create the other inverter, you can copy the cell view and modify the transistor sizes. Copying a cell view is done by right-clicking on the cell name and selecting copy. The copy cell popup will show, allowing you to name the new cell in the To section. Hit OK and a Message will popup saying the files are copying. Alternatively, assign a parameter variable for the widths and modify the widths in the test bench (see the end of this tutorial).



30. Next we will make a test bench to simulate our NAND gate. Create a new Cell View in the Lab1 library called **testNAND**.



31. Since we wish to test the NAND gate we just created, we must add it to the schematic. Add an instance of the NAND symbol from the Lab1 library. (From now on, this selection sequence will be given as: **lab1 -> NAND -> symbol**) Click Close. Place the NAND gate in your blank Virtuoso window and then press Esc to leave the add instance mode.



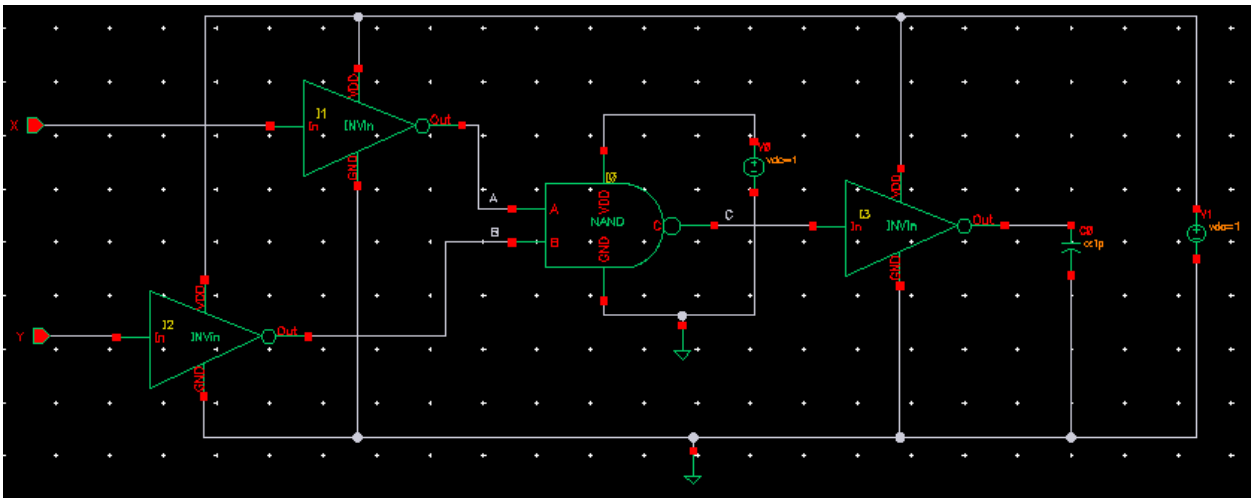
32. Add the input invertors and output inverter to your test bench. (**lab1 -> INVin -> symbol and lab1 -> INVout -> symbol**)

33. Add the output load for the output invertor. We will use a single capacitor for this (**analogLib -> cap -> symbol**)
34. Now that you have placed the cells you have created in the schematic, you need to add power and input sources. For the power source(s), you can place a dc voltage source in the schematic by adding the vdc cell from the analogLib library (**analogLib -> vdc -> symbol**). Remember to set the DC voltage in the properties (the 65nm kit we are using, uses a standard Vdd of 1.0 V)! Alternatively, you can add the vdd symbol from the analogLib library (**analogLib -> vdd -> symbol**). When using the vdd cell, the voltage must be set in the stimuli properties (more on this later).

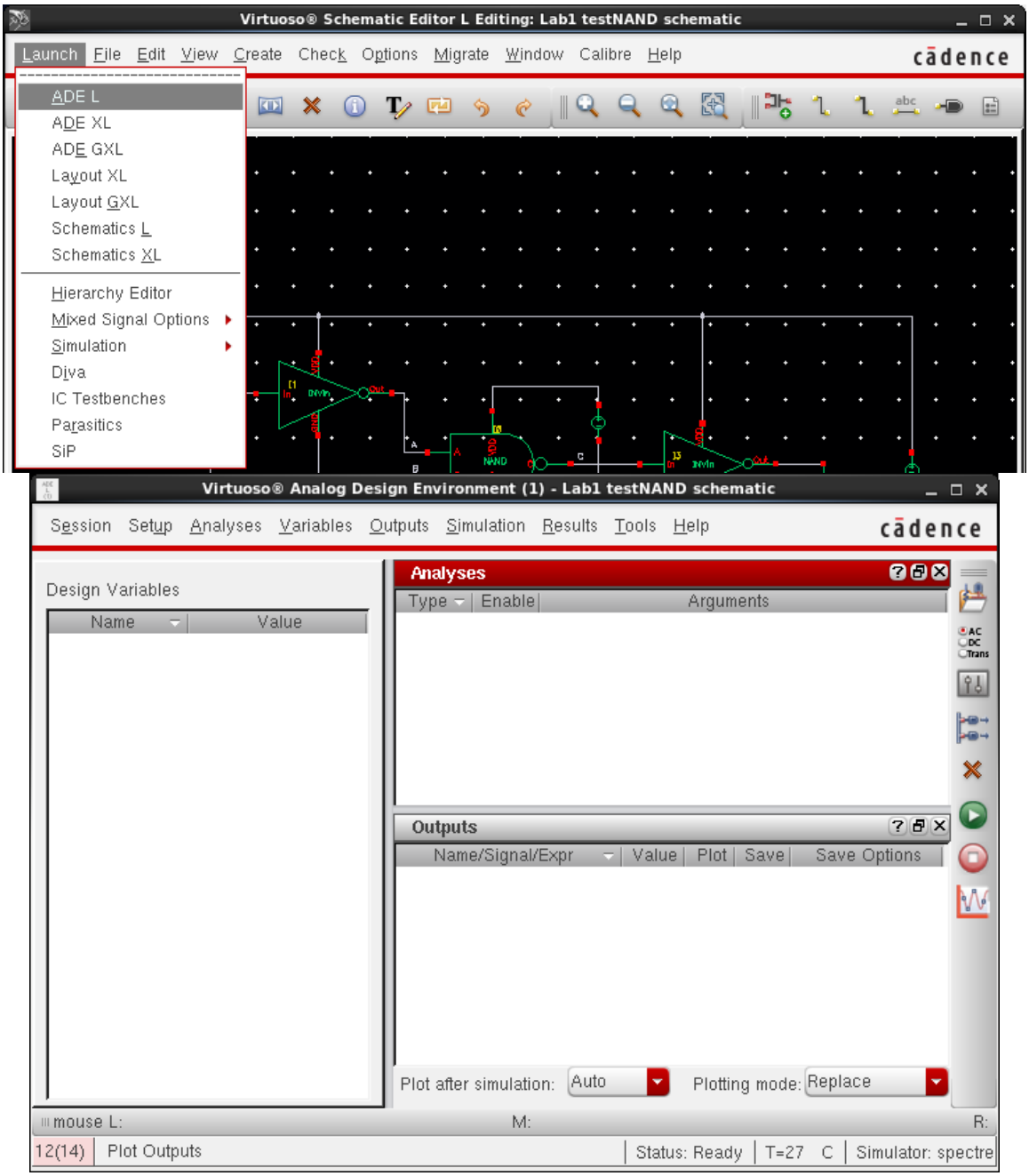
    There can only be 1 vdd voltage in a design, but there can be as many vdc sources as you want. However, because of this, rather than having VDD and GND pins (as you did when you created your NAND gate) you can use the vdd and gnd symbols from the analogLib library. Thus, the generated symbol will not require you to manually connect the VDD and GND signals. Instead, when you set the global vdd stimuli, it will set the voltage for anything connected to the vdd cell symbol.
35. Connect all Grounds to the gnd cell from the analogLib library. Generally this means connecting the '–' terminal of voltage sources to gnd as well. Not doing so may result in an unexpected output.

36. For the inputs, you have 2 options. You can either simply add the voltage sources from the analogLib library to your schematic (you will probably need **analogLib -> vbit -> symbol** and **analogLib -> vpulse -> symbol**), or you can you an input Pin and specify the input using stimuli. The advantage to the latter case is that you do not need to modify your schematic when you need different inputs. Instead, you just change the simulation. This allows you to easily save and load different simulations to redo previous simulations. To do this with the former case you need to save multiple versions of the schematic. Since, we need different input sources in this lab, **insert pins X and Y for the inputs**.
37. Now that we have everything needed in our schematic, we need to wire it up. Select wire (narrow) and connect all the symbols. If you need to pan around, use the **cursor arrow keys**. Using **Ctrl + scroll** will zoom in and out. **Shift + scroll** will pan left and right. Alternatively, you can zoom with the Zoom In  and Zoom Out  buttons on the toolbar. Hitting the '**z**' key, or Zoom to Selected  buttons on the toolbar, will allow you to draw a box around the area you want to zoom in on. The Zoom to Fit  button on the toolbar will Zoom to fit the entire schematic in the window.

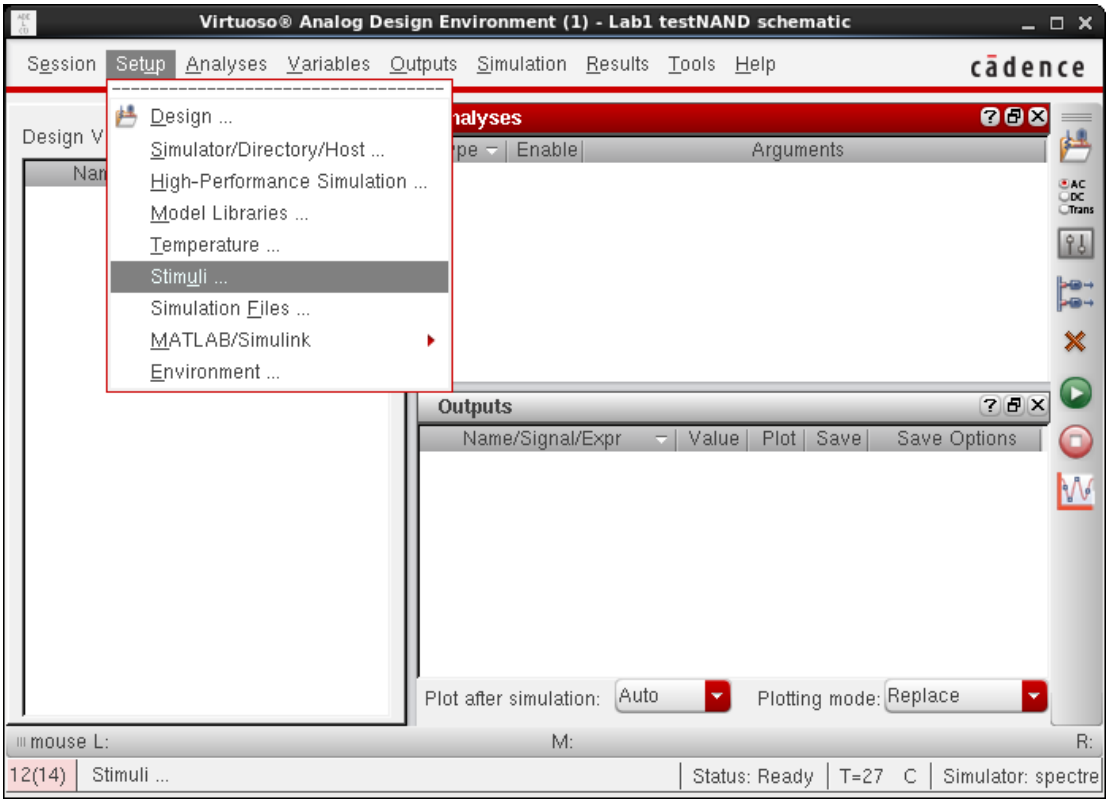
38. Your design should look similar to the one below.



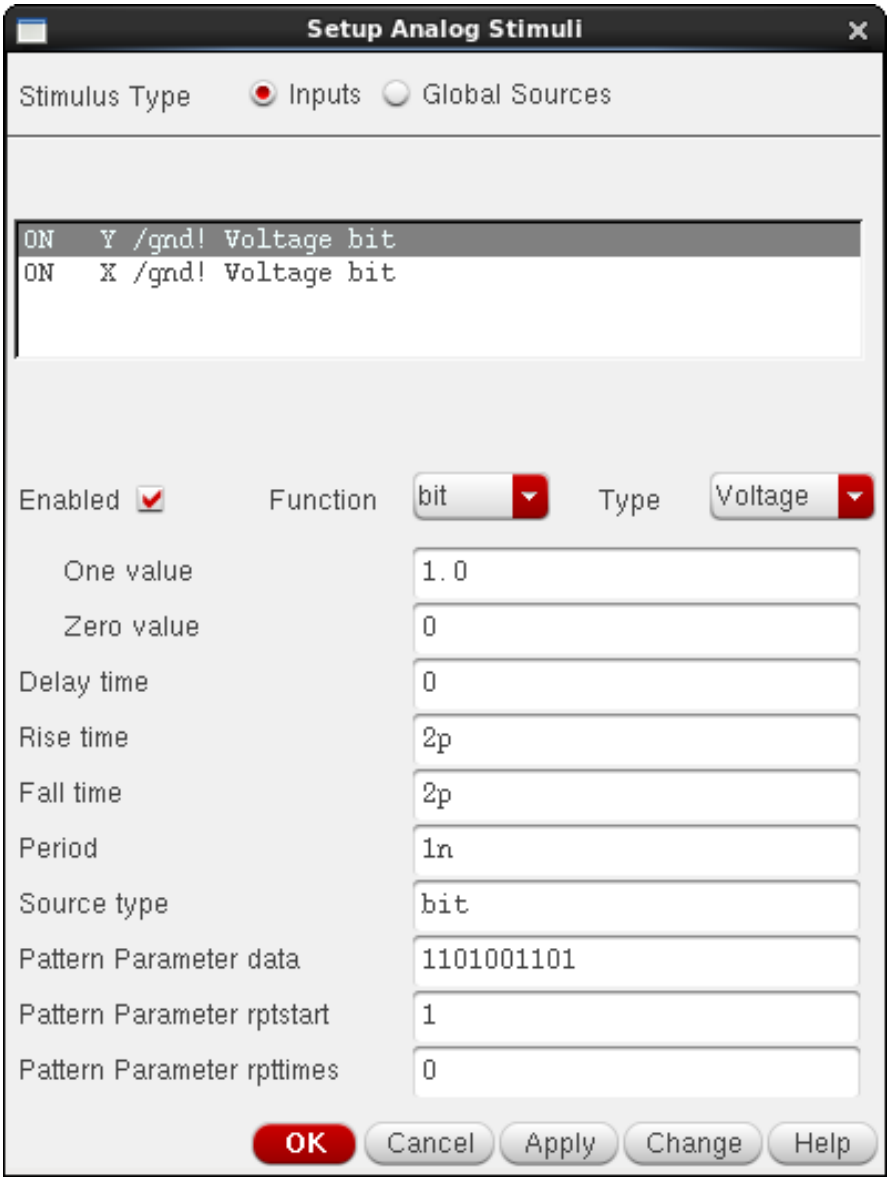
39. Before we move on, lets name the A, B, and C wires so we can easily identify the inputs and outputs when running simulations. This can be done by hitting the Create Wire Name button, hit '**L**' (lowercase) on the keyboard, or select it by going to **Create->Wire Name…** on the menu Bar. The Add Wire Name dialog box will popup. In the Names field type "A B C" (with spaces between the letters). Now click the wires you wish to name (in the order than you typed the names). Name the wire connected to pin A on the NAND gate, A. The wire connected to Pin B should be named B, and the output should be named C. (see above)
40. Now that the schematic is setup, lets setup the simulation. To simulate the design, we will be using the Analog Design Environment L. Click **Launch -> ADE L** on the menu bar to launch the Virtuoso analog design environment.



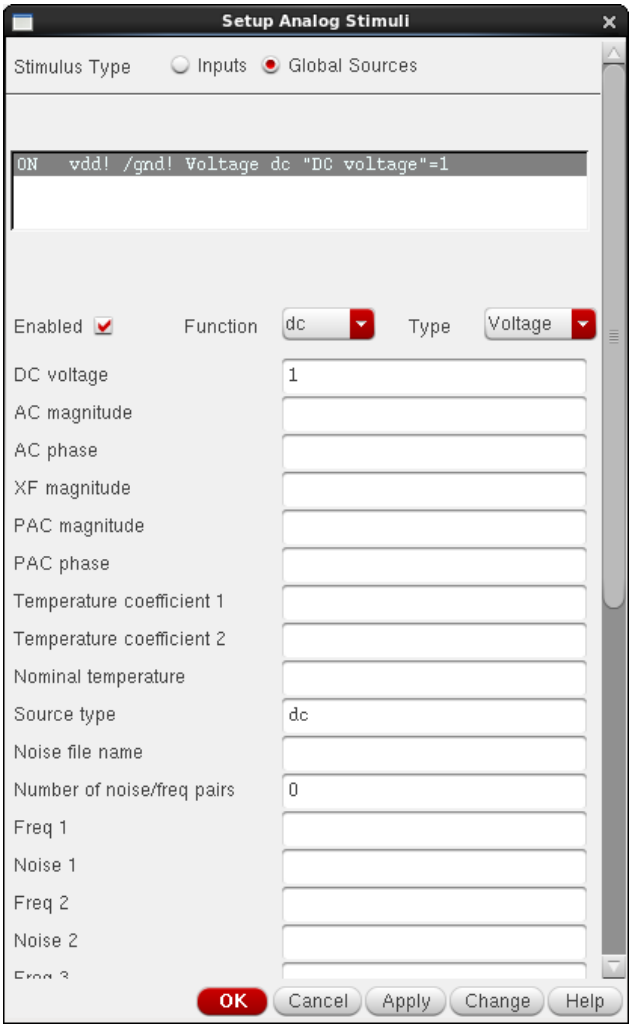
41. Before we setup the analyses, lets setup the input stimuli. To do this, go to **Setup -> Stimuli**



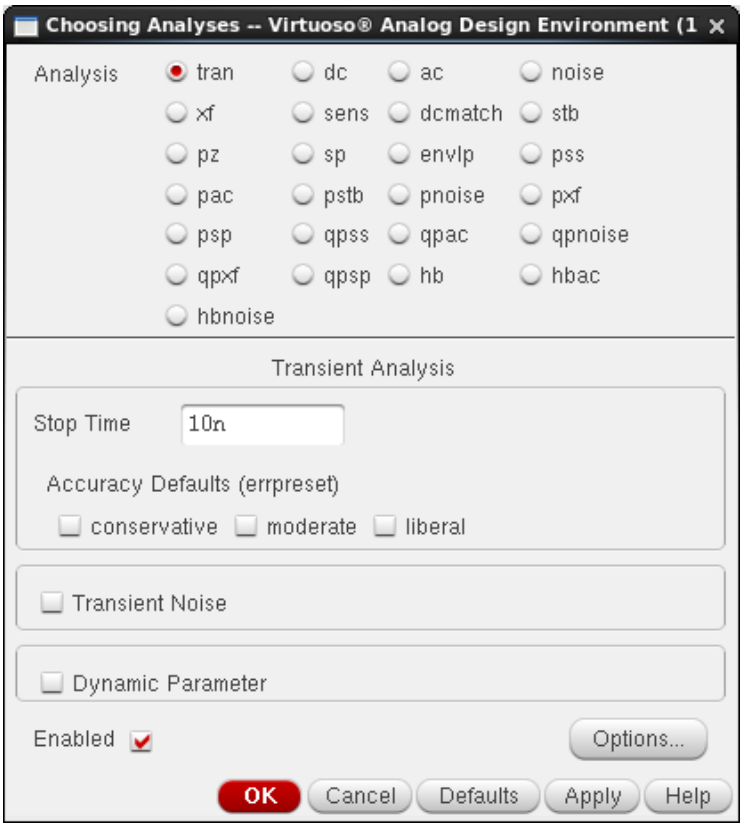
42. The stimuli dialog box will popup. You should see the X and Y pins in the input stimulus Type. For Part 2 of the lab, you will probably want to use a voltage bit source. To do this, select bit in the function pull down menu, check the “Enabled” check box, set the One Value to Vdd (1.0 V), Zero Value to 0, Delay time to 0, Rise time to 2p, Fall time to 2p, and period to 4n. The Bit pattern you wish to test is set under “Pattern Parameter data”. Hit “Apply.” Now that the first input is setup, setup the next one with the same parameters. Always hit “Apply” before changing input sources. Hit OK when you are done. Remember that X and Y are the opposite values of A and B.



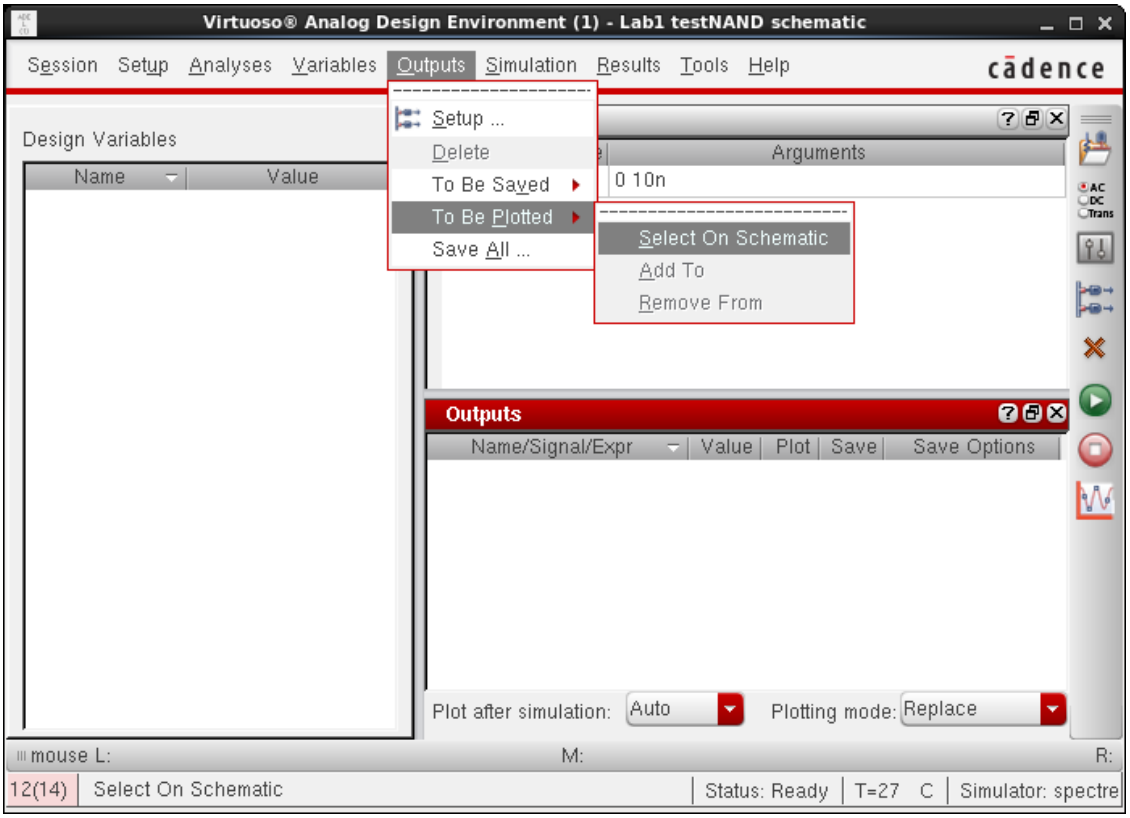
(aside)
If you used the “vdd” cell from analogLib, you would set it’s voltage in the Global Sources Stimulus Type.



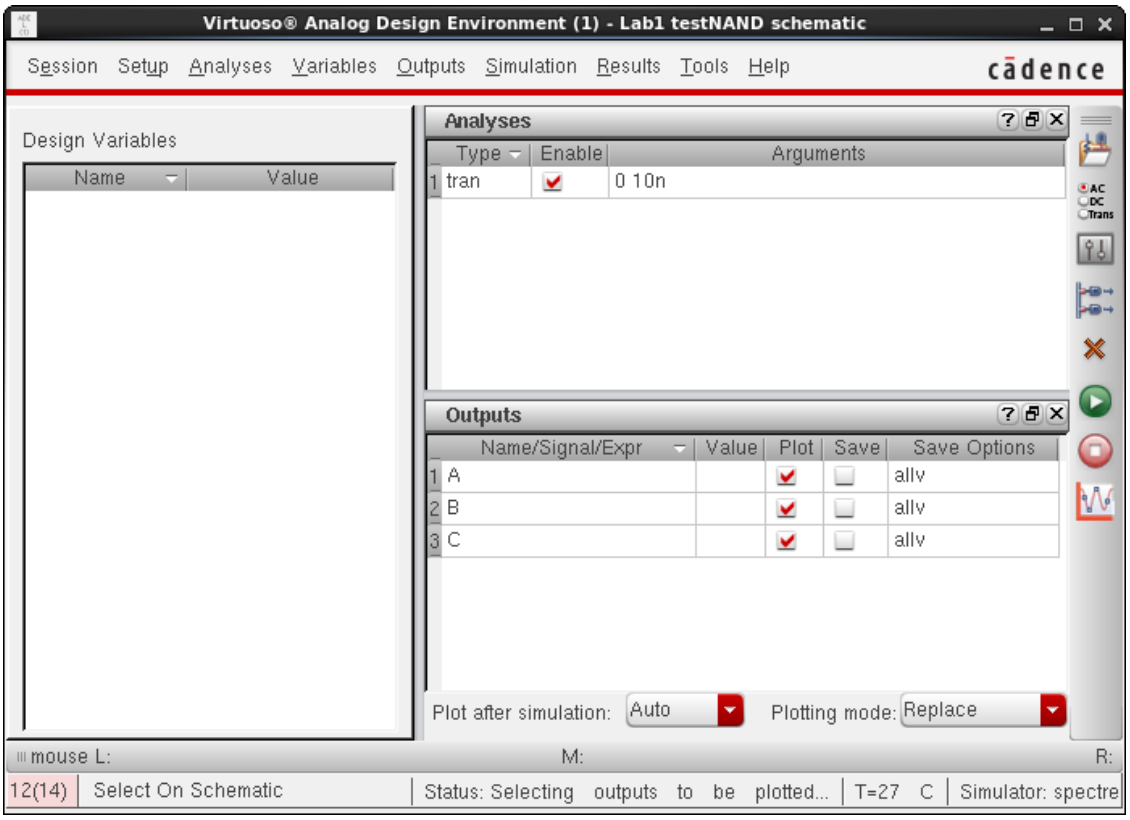
43. Now lets setup the simulation analyses. Click on **Analyses -> Choose** in the menu bar. The Choosing Analyses dialog box will show up. Select Analyses type as tran and enter 10n in Stop Time field and select Enabled. Click OK.



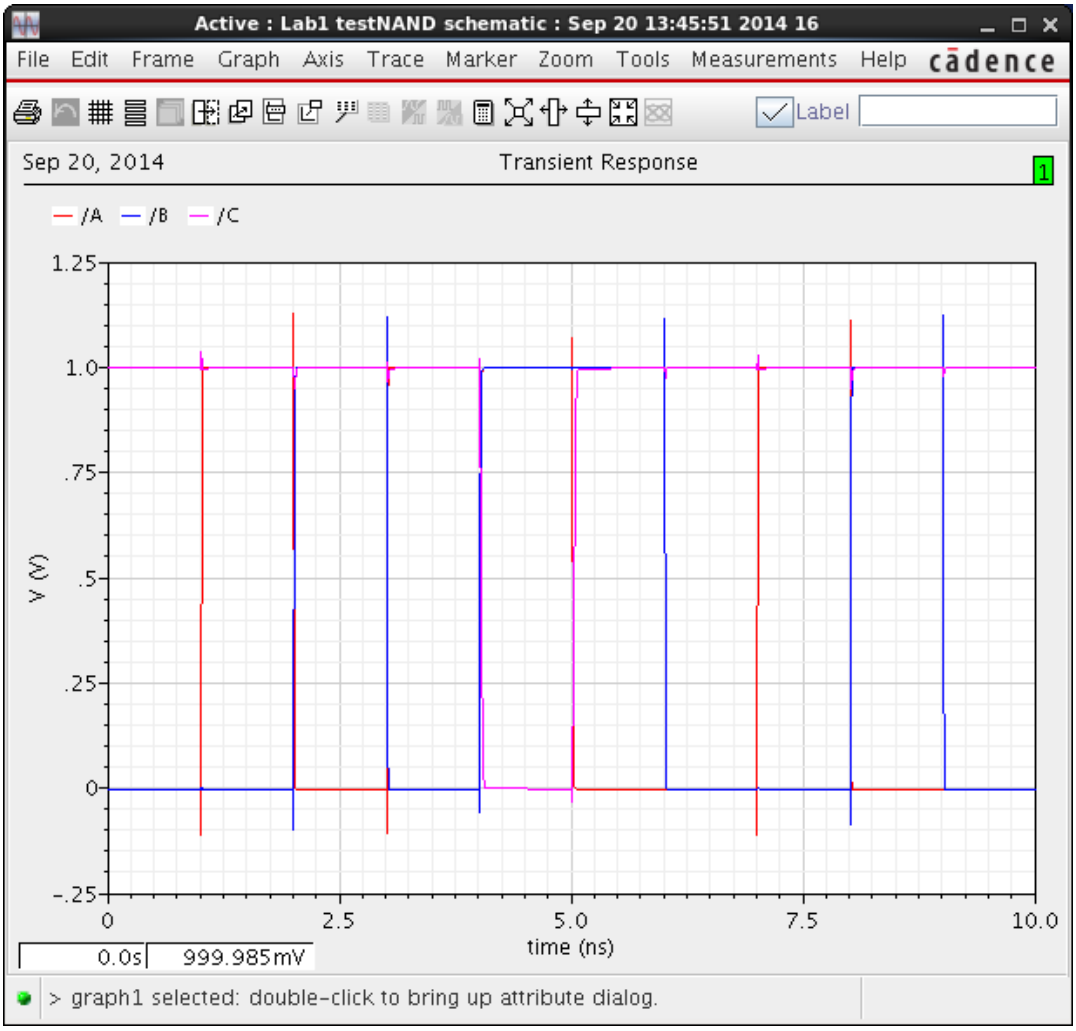
44. Now that the analyses is setup, we have to select the signals we wish to plot. Click on **Outputs -> To Be Plotted -> Select On Schematic** in the menu bar. The schematic view should be brought to the front. Click the input wire connected to A, the input wire connected to B, and the output wire connected to C. The selected wires should be highlighted in a colour. This colour corresponds to the colour of the signal in resulting plot.



45. Now your Virtuoso Analog Design Environment should look like the following figure.



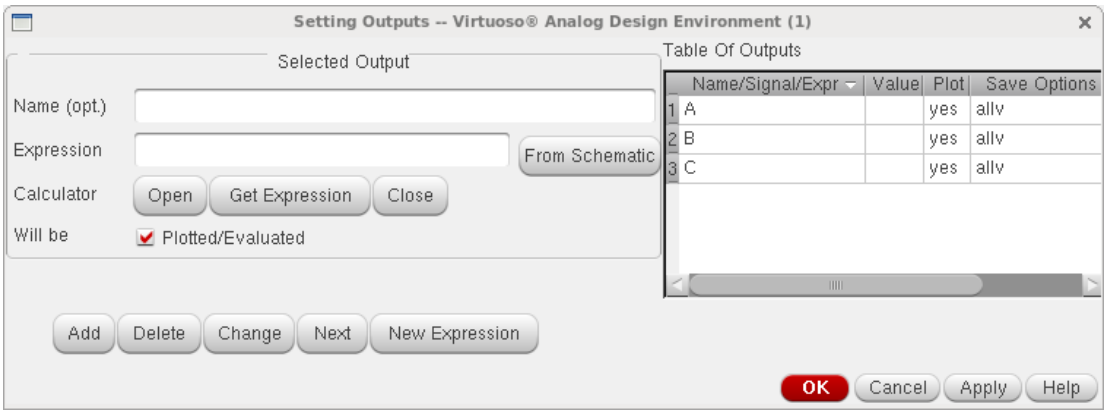
46. Click **Simulation -> Netlist and Run** in the menu bar, or click on Netlist and Run  on the right side. A message box should open and show log file. If the simulation is successful, input/output waveforms will be shown in a new window.

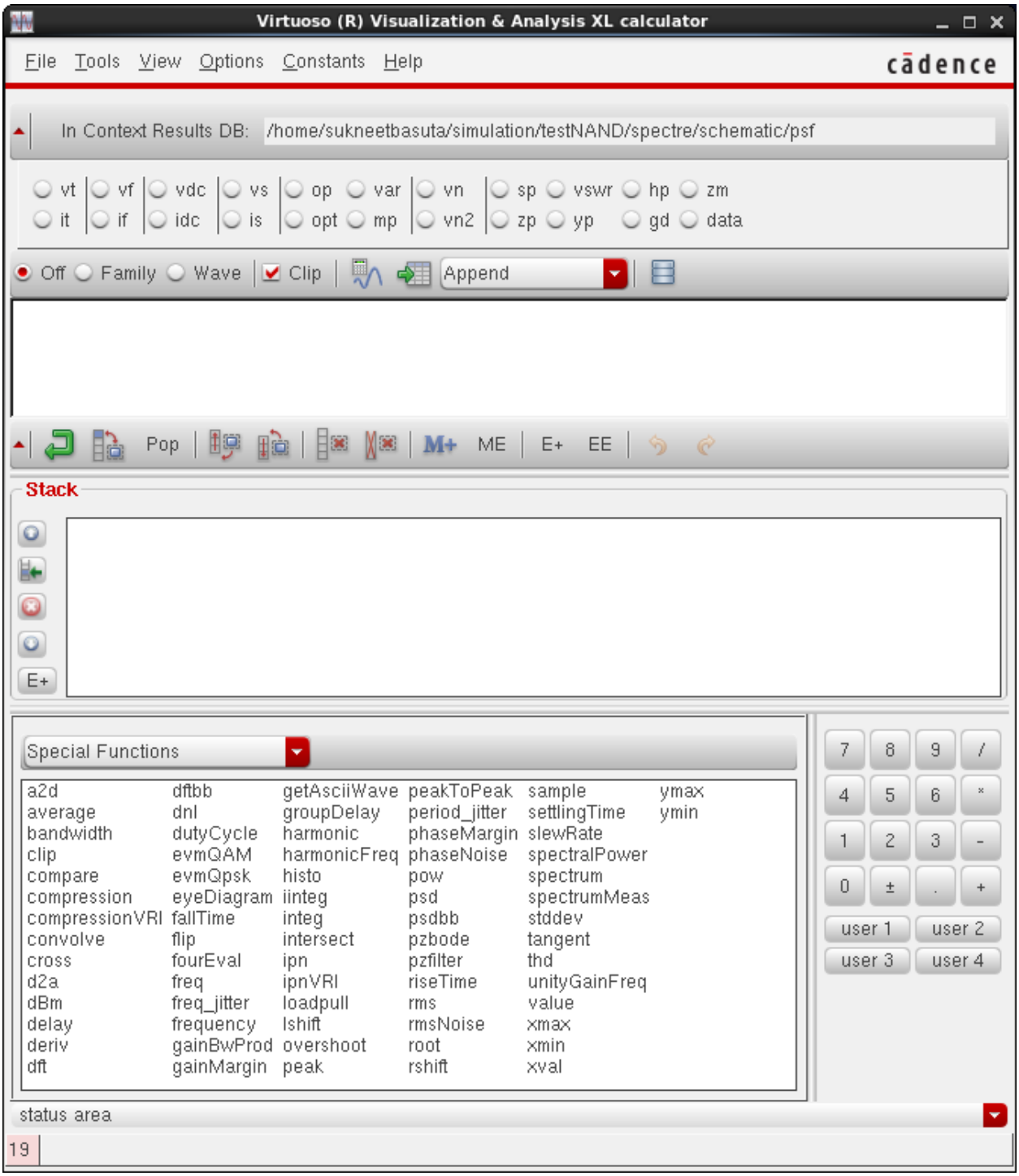


47. To see the waveform separated, select **axis -> strip**, or click on Strip Chart Mode  on the top toolbar.
48. There is 2 ways you can find the delays.

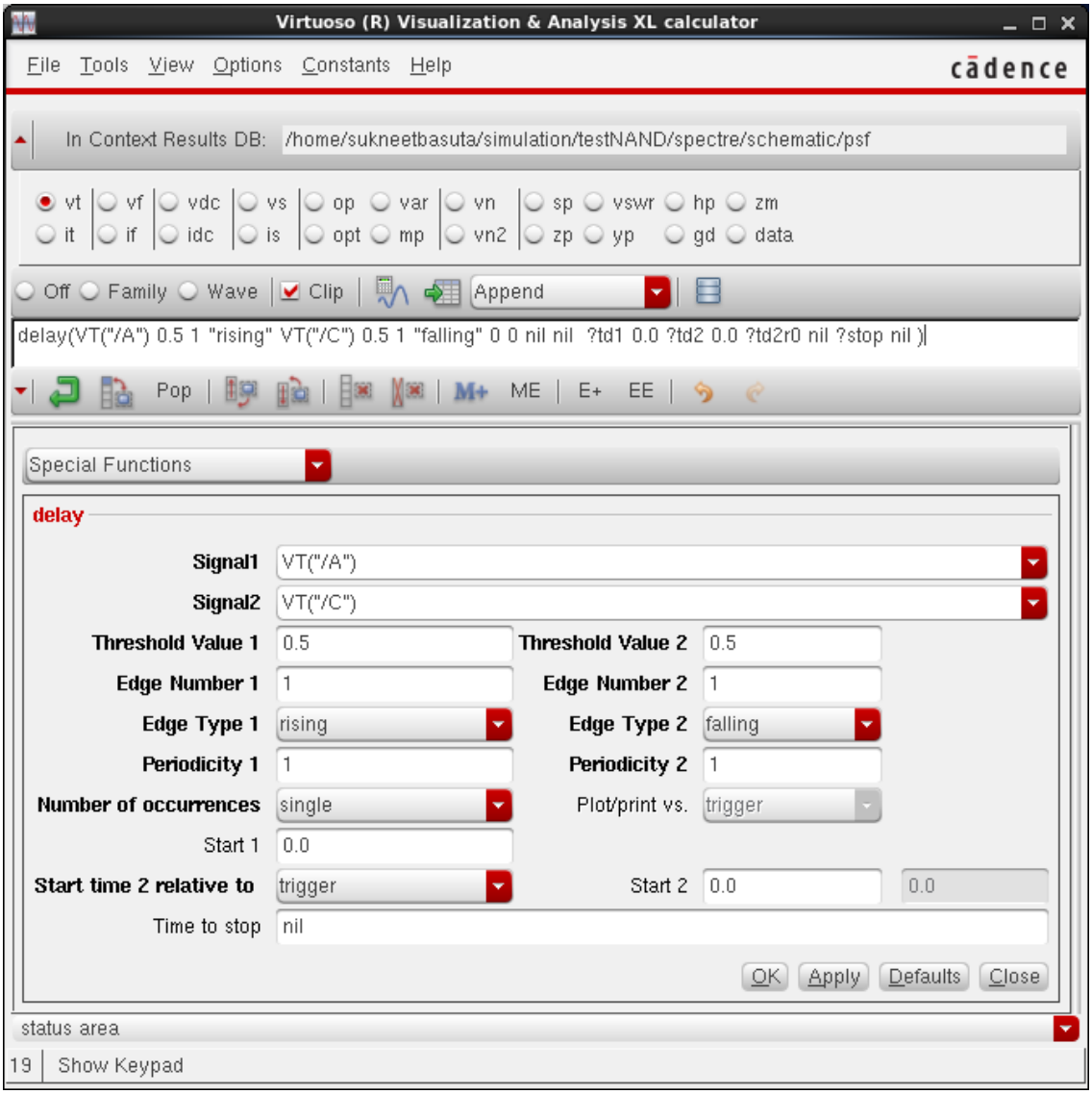
    To find delay manually, look at transistors of output and the corresponding input causing the transition. For example, in this case, the first output transition is at around 4 ns. To find exact value at 50% output (0.5 V), you can use Trace marker (under Marker -> Place) and click at 0.5 V crossing of the waveform. It is show the corresponding time. To change where the marker is located select the marker, and then choose Marker -> Edit, now you can use the X, Y, or XY modes to change the location. You can also delete the marker and place a new one. You can find the difference between 2 markers by selecting Marker-> Add Delta and selecting the markers.

49. The better and more accurate way to find the delays is to have cadence automatically find the delays. To do this we use the Calculator. If you only wish to find the delays after a simulation is run, you can open the calculator by going to **Tools->Calculator** in any ADE window. However, this will be tedious if we are doing more than 1 simulation. Instead, lets have Cadence automatically get the delay whenever the simulation is run.
50. To do this, in the Analog Design Environment window, select **Output->Setup** (or right-click the Outputs mini window in the Analog Design Environment window and click on Edit). The Settings Outputs dialog window will popup. If a signal is already selected, click on New Expression. Clock on Open beside calculator to open the calculator.



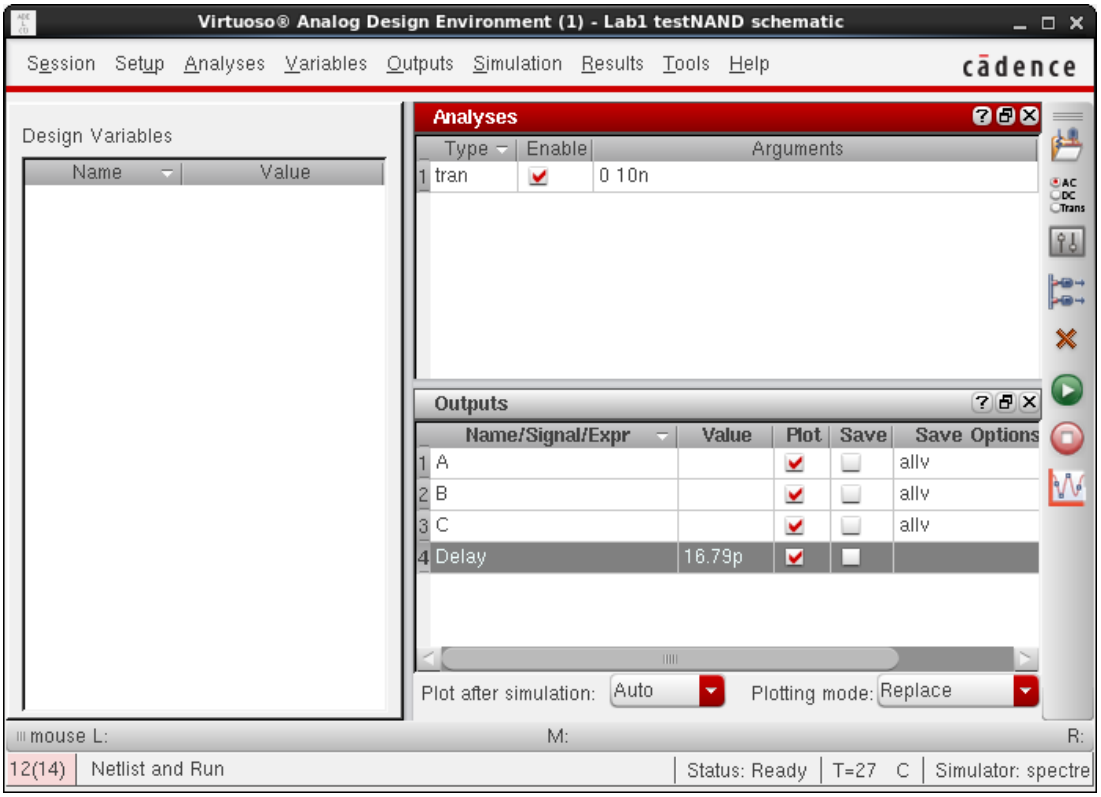


51. The Calculator is a very powerful tool with many functions. However, for now we are interested in the delay. Click on delay in the functions list at the bottom.

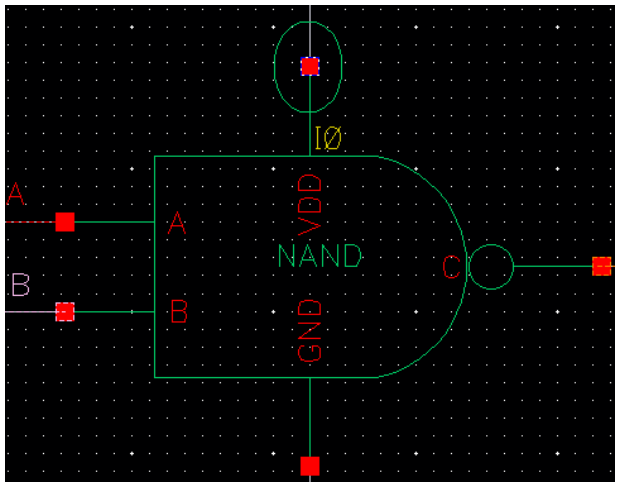


Place the cursor in Signal 1 box and click Vt (for transient analyses). The schematic window should pop up. Select wire A. Place the cursor in Signal 2 box and click Vt again. The schematic window should pop up again (if it does not, select it and then select Vt again). Select wire C. Change Threshold value 1 to 0.5 (i.e. 50% of Vdd). You can choose edge type (rising, falling, either) and Edge Number, so that any combinations of rising and falling can be found. Change Threshold value 2 to 0.5. Click Apply. Go to Setting Outputs window and click Get Expression. Give a Name of the expression. Click Add and then OK. Run the simulation and you will see the calculated value in the Outputs mini window.

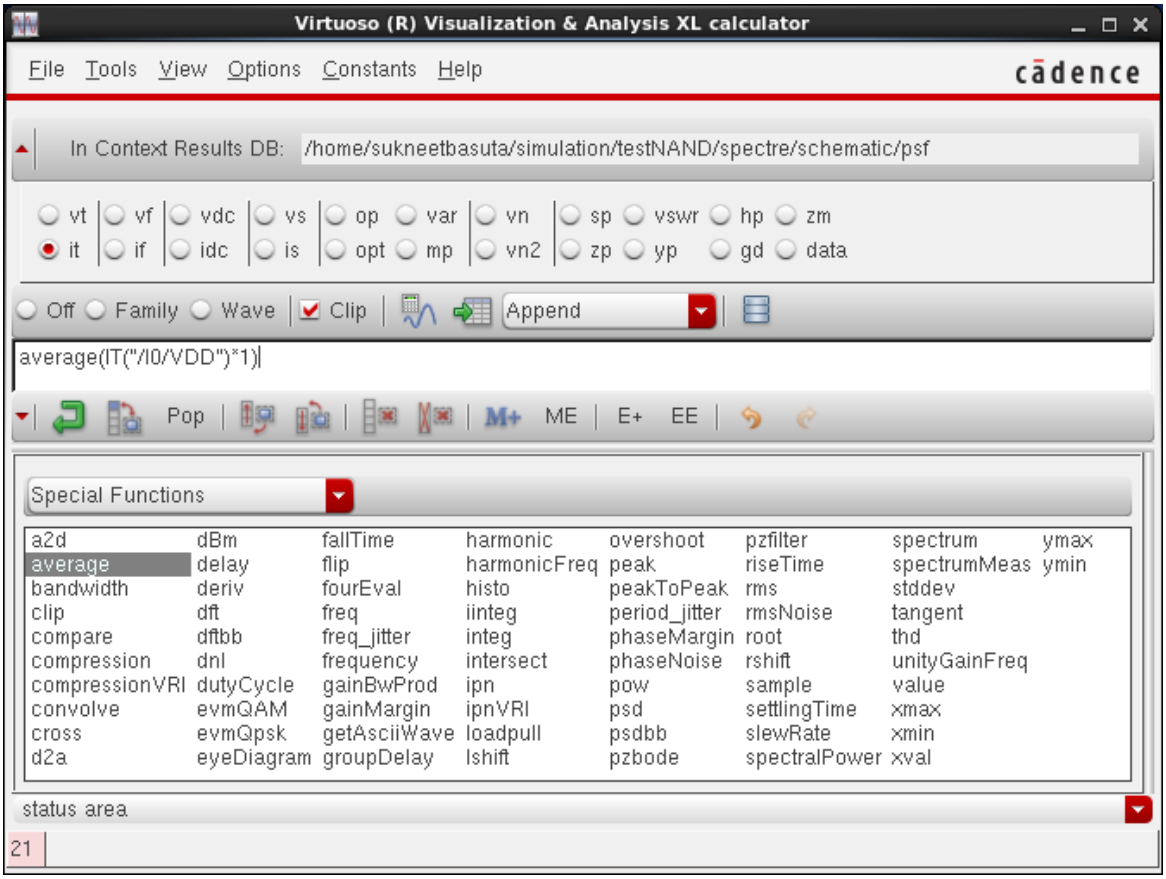
If you simply wish to evaluate the expression, hit the Evaluate the Buffer  button in the calculator.



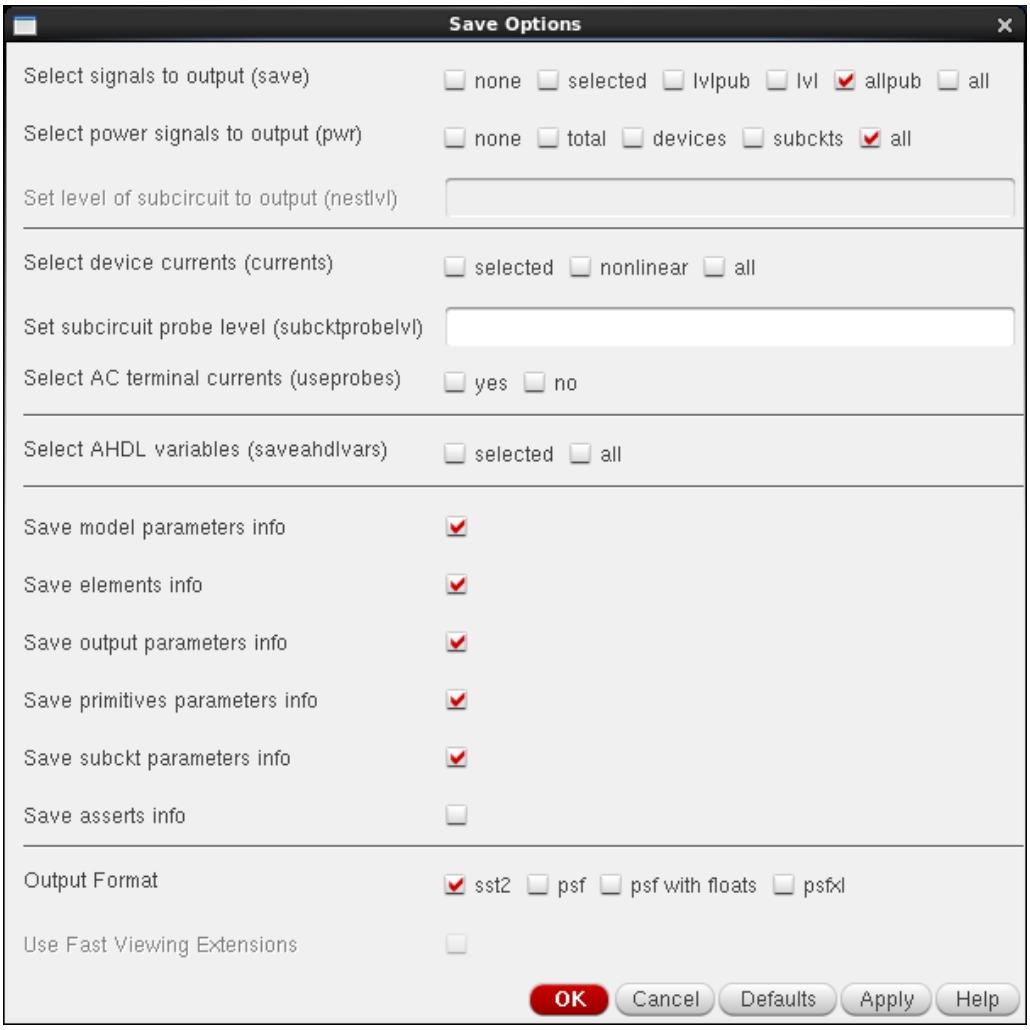
52. You have 2 options on finding the average power. You can find the current supplying the NAND invertor and multiply it by Vdd, or you can have Cadence directly tell you how much power each device is consuming (see next step).
    The former method can be done by adding a output to be plotted (or saved) and click on the VDD node of the NAND gate (the red pin). A colored circle will encircle the selected node, indicating you are measuring the current going through that node. Alternatively, you can select the node in the calculator by selecting 'it' (for transient analyses) radio button. This measured current is the instantaneous current at a given time.



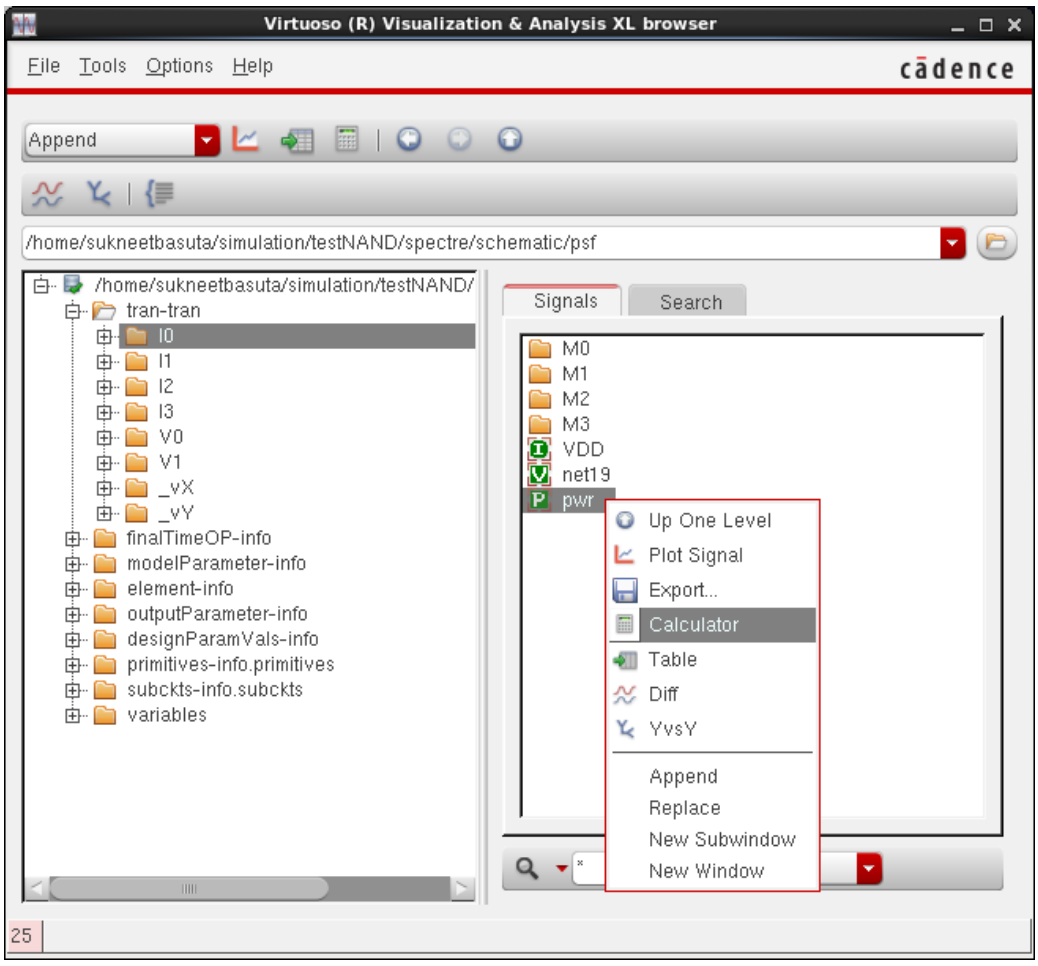
To find the average power, open up the calculator, and use the average function to average the I* V expression.



53. The arguably better way to find power is to have Cadence directly tell you the amount of power consumed. The advantage to this method is you can see exactly how power each individual device and transistor is using very easily.
    Select Outputs->Save All … to open the Save Options window. In this window, check the all button next to “Select power signals to output (pwr)”. Select all tells Cadence to save all power signals. (total only save the total consumed power of the entire schematic and devices only save power for each individual device) Select Ok.



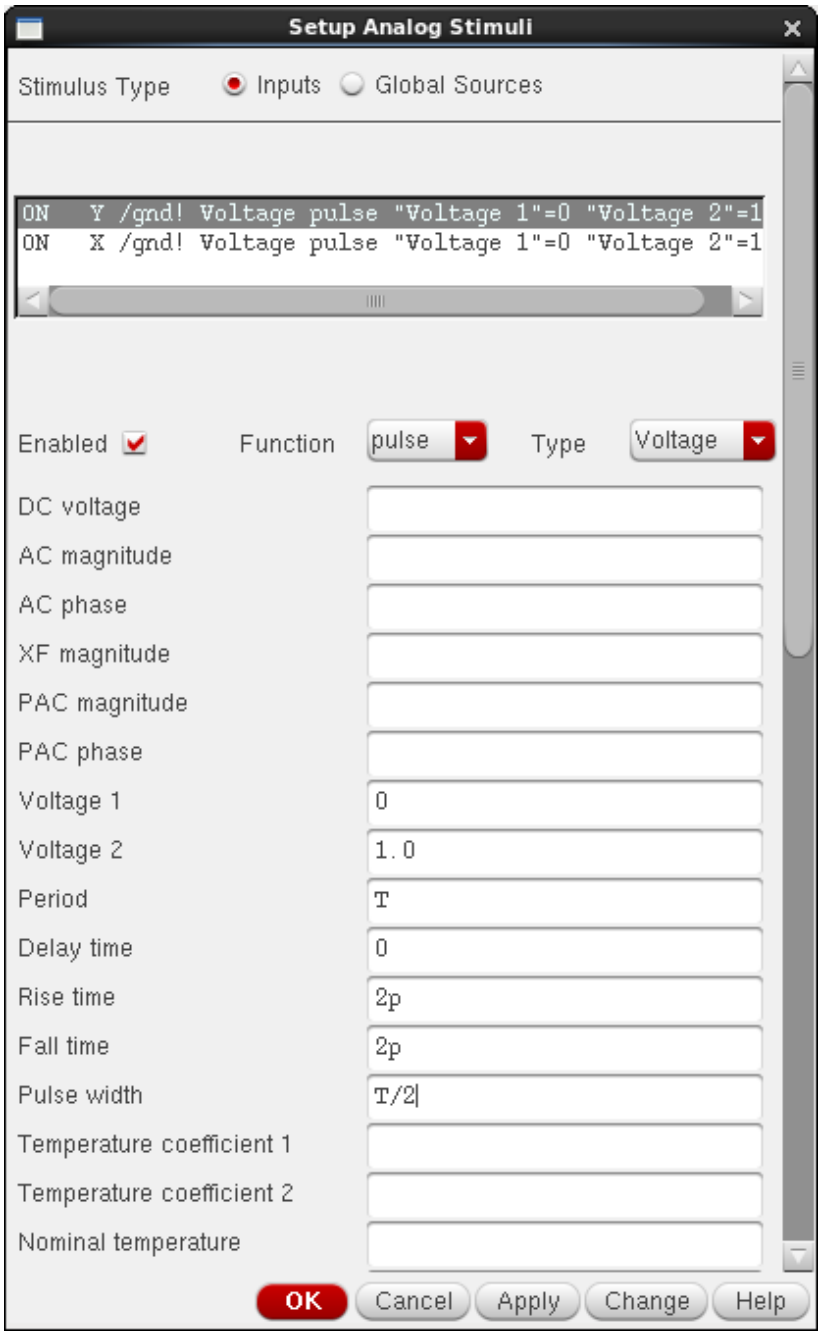
Now run the simulation. To see the power signals you need to view them through the Results browser. Access the Results Browser by clicking on **Tools -> Results Browser** (or **Tools -> Browser** if you are in the plot window). Since you are running transient simulations, all the simulation results will be in the **tran-tran** folder. In this folder you will see I0, I1, etc folder and all the wire names in your schematic. You should also see ":pwr" in the list. This is the total power of all the devices in your schematic. You can click on any signal to see the simulation results. To find the power consumption of your NAND device, look at your schematic to find the device (or Instance) name. For example, in step 53, the NAND device has a device name of "I0". In the Results Browser, select the folder with the device name. You should see a "**pwr**" signal. This is the instantaneous power consumed by that device.



To find the average power, right click the pwr signal and select Calculator. This will open up the calculator with the expression for the data. Use the average function to average the pwr signal.

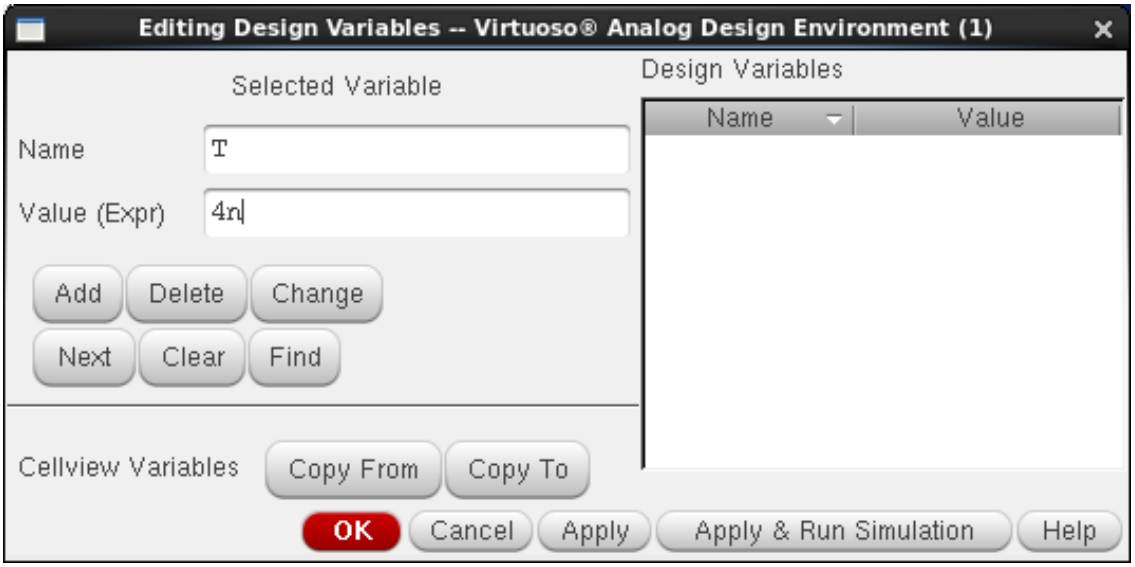
54. Part 3 of the lab requires both inputs to be connected to pulse waves. To do this, go back into the Setup Analog Stimuli dialog box (Setup -> Stimuli) and change the input functions to “pulse”. Use a rise and fall time of 2p and 0 delay. You will most likely want the Pulse width to be ½ of the period. Since you are required to sweep the input frequency, enter a variable in the period field. You will need to specify a value for this variable before running a simulation. For example, you can enter “T” in Period field, “T/2” in Pulse width. Then during simulation, specify T=2n.

    Note that you can also enter a variable or expression in any field and later assign a value to that variable during simulation.

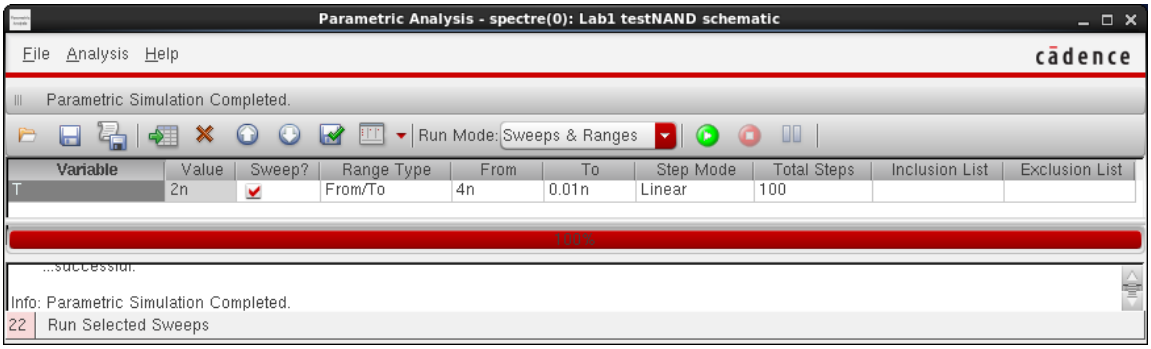


55. To assign values to variables in your schematic, first we must copy the variable from the cellview. Click on **Variables-> Copy from Cellview**. You should see all available variables in the Design Variables mini window in the analog design environment. Click on the values column to assign a value to the variable (alternatively, right click the variable name and hit Edit).

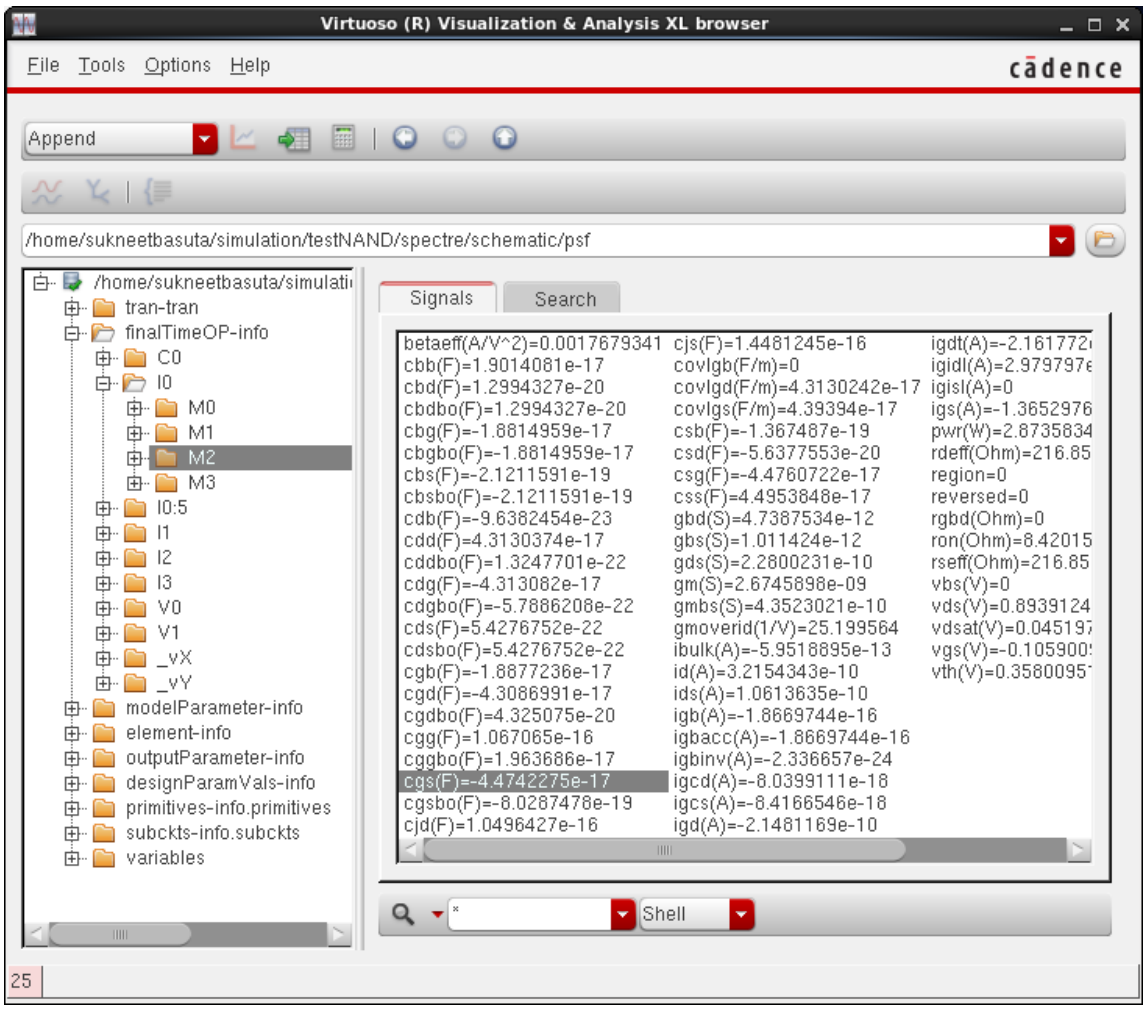
    Variables used for stimuli will not be automatically copied. You need to manually add them. To do this, click on **Variables -> Edit** to open the Editing Design Variables window. Type in the variable name you used, assign it a Value, and Hit Add. Hit Ok to close the window.



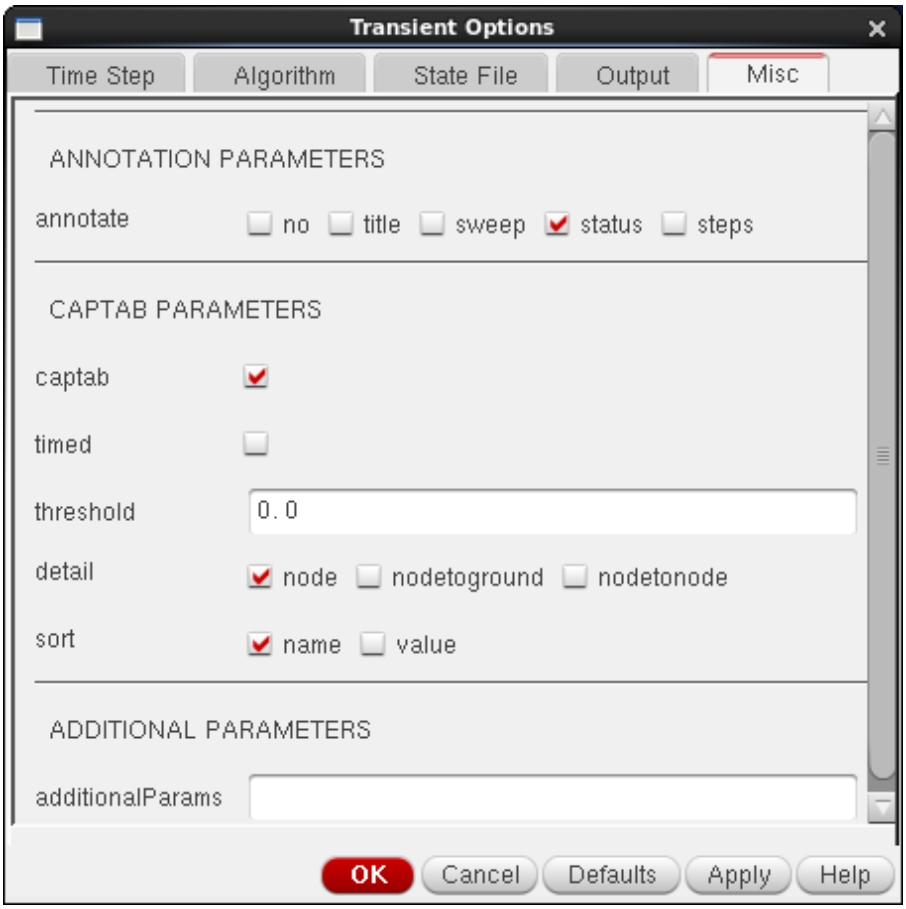
56. The above works when we only want to assign 1 value to a variable. However, we need to sweep the variable to test many different values. A Parametric Analysis will accomplish this. Open the Parametric Analysis window by selecting Tools-> Parametric Analysis. In the Variable field, type in the variable you wish to sweep, or select it from the drop down list. In the From and To fields, put the values you wish to sweep from and end at. In the Step Mode you can select how you wish to sweep the variable. Auto will have cadence decide on a appropriate number of steps. Linear will allow you to choose the total number of steps. Linear Steps allows you to specify the step size.



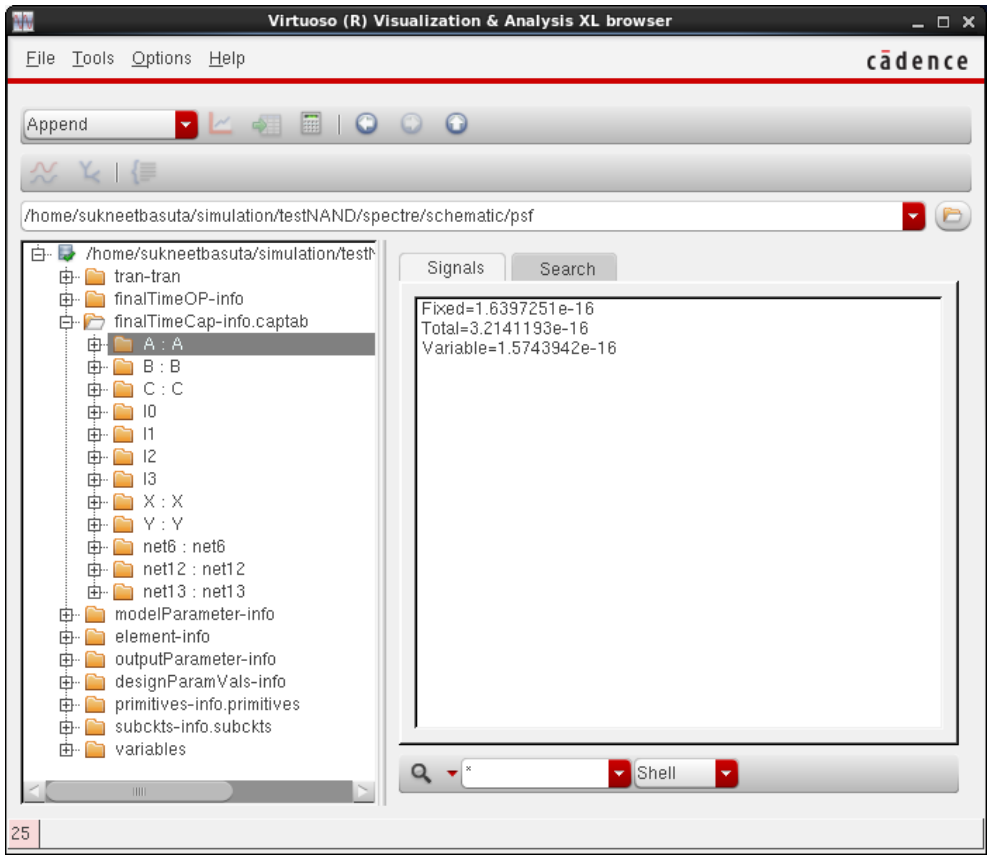
57. Click on the Run Selected Sweeps  button on the top toolbar (or click on Analyses -> Start All) to run the parametric Analysis. Make sure that your transient analyses is long enough for the longest pulse period you specified!
58. Finding the capacitance at a node can be estimated by adding all the output capacitances of a gate + the load capacitance (which maybe the input capacitance of another gate). You can find each intrinsic and extrinsic capacitances of a transistor by going to the results browser and selecting **finalTimeOP-info** rather than tran-tran. finalTimeOP-info is the results at the completion of the simulation. If you entire the device folder and click on the transistor name (i.e. M2), you will see all it's model parameter info.



59. An easier and more accurate way to find the capacitances at a node is to use captab. To enable captab, open the Choosing Analyses window (**Analyses->Choose** ,or right click the analysis in the Analyses mini-window and select Edit). Click the Options button on the bottom right. The Transient Options window will popup. Select the Misc tab and check the captab checkbox. You will see 3 levels of detail: **Node** will state the total capacitance at a node, NodetoGround will list the capacitance to ground, and NodetoNode will list the total capacitance between every 2 nodes. Hit Ok to close the Options window and then hit OK again in the Choosing Analyses window.

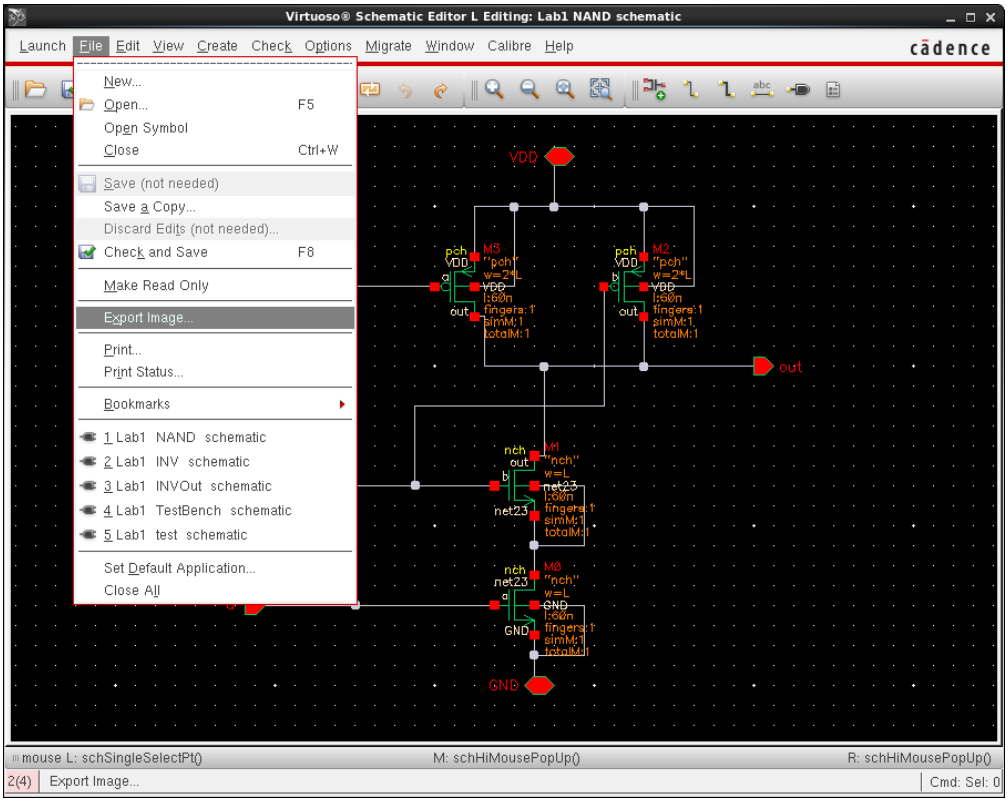


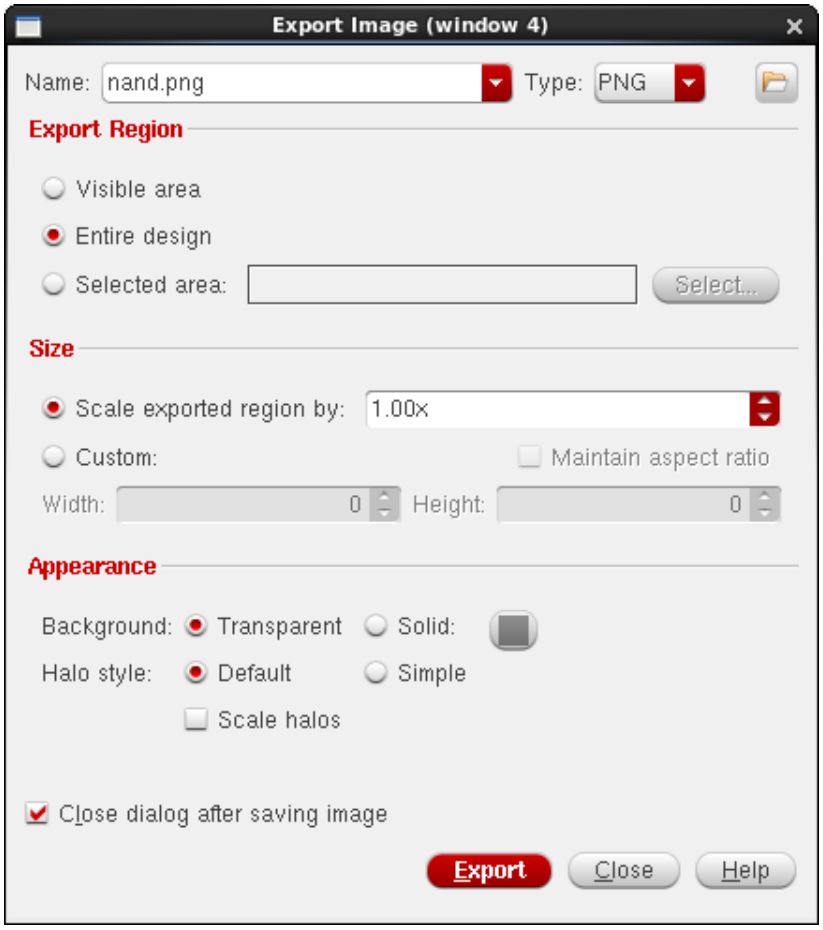
Access the Node capacitances is then done in the results browser. In the Results browser, select the **finalTimeCap-info.captab** folder and then the folder of the Node's name. You will see a Fixed, Total, and Variable capacitance listed here.


Virtuoso (R) Visualization & Analysis XL browser
File Tools Options Help
cadence
Append
/home/sukneetbasuta/simulation/testNAND/spectre/schematic/psf
/home/sukneetbasuta/simulation/testN
tran-tran
finalTimeOP-info
finalTimeCap-info.captab
A : A
B : B
C : C
I0
I1
I2
I3
X : X
Y : Y
net6 : net6
net12 : net12
net13 : net13
modelParameter-info
element-info
outputParameter-info
designParamVals-info
primitives-info.primitives
subckts-info.subckts
variables
Signals
Search
Fixed=1.6397251e-16
Total=3.2141193e-16
Variable=1.5743942e-16
Shell
25

Helpful hints for lab 1 part A:

- If you want to find out what is inside a symbol, select it and press **"Shift-X"** or **"x"** (lower case X) to **descend** (first one lets you edit, second one only to view as read only). Alternatively, right click the symbol and select Descend. Press **"Ctrl-X"** when you are done to **ascend** to the top level.
- You can save your settings of Analog Design Environment by selecting **Session -> Save State**. To load a previously saved state, select **Session -> Load State**.
- Anytime you make any change in schematic window, save it before you simulate it.
- To make certain parameters of instances changeable (e.g.: make an inverter in which you can change the nMOS and pMOS widths between instances) use **pPar("varname")** in a property of an object in the instance schematic, where varname is the name that will be shown in symbol attributes, accessed in a higher level. For example, in your inverter schematic, set value for nMOS and pMOS width as pPar("InvWidth"). Then create the symbol. Now, if you place this inverter symbol in another higher level schematic, when you select the inverter and view it's property (by pressing 'q'), you should notice a new variable at the bottom named InvWidth. You can assign a different value for same symbol in different instances.
- Delay measurements should be done in transient analysis mode. Make sure A and B matches given wave shape (not X and Y). Look closely at your graph for rise times and fall times (You should be able to find all cases as required from this plot) and tabulate them. Find propagation delay (maximum) and contamination delay (minimum) from the table.
- Use variables for defining widths of MOSFETs, so that you can change them from the Analog Design Environment during simulations keeping β constant.
- You can save an image of the schematic by going to **File-> Export Image.** The Export image window will popup. Give the image a name, select "Entire Design" under "Export Region", and hit export. This will save the image to the folder you created in Step 1. Hitting the open folder icon on the top right will allow you select a different location.


Virtuoso® Schematic Editor L Editing: Lab1 NAND schematic
Launch File Edit View Create Check Options Migrate Window Calibre Help
cadence
New...
Open... F5
Open Symbol
Close Ctrl+W
Save (not needed)
Save a Copy...
Discard Edits (not needed)...
Check and Save F8
Make Read Only
Export Image...
Print...
Print Status...
Bookmarks
1 Lab1 NAND schematic
2 Lab1 INV schematic
3 Lab1 INVOut schematic
4 Lab1 TestBench schematic
5 Lab1 test schematic
Set Default Application...
Close All
VDD
GND
out
mouse L: schSingleSelectPt()
M: schHiMousePopUp()
R: schHiMousePopUp()
2(4)
Export Image...
Cmd: Sel: 0


Export Image (window 4)
Name: nand.png
Type: PNG
Export Region
Visible area
Entire design
Selected area:
Select...
Size
Scale exported region by: 1.00x
Custom:
Maintain aspect ratio
Width: 0
Height: 0
Appearance
Background: Transparent Solid:
Halo style: Default Simple
Scale halos
Close dialog after saving image
Export
Close
Help