Assignment 1
Instructor: Maitham Shams

ELEC-4708A Advanced Digital ICs, Fall 2014
Department of Electronics, Carleton University

Student Name :
Student ID :

Mark :
Out of : 100

---

1. <25 marks> Implement $F = \overline{(AB + C)D}$ in Conventional CMOS. Assume a 65 nm technology. Note that since parts "a" and "b" can also be done independently, your mistake in "a" is not carried forward to "b".
   a. Draw the most efficient schematic
   b. Draw the most efficient stick layout diagram
   c. Estimate the area in micron square

2. <25 marks> Implement the XOR function $Z = A \oplus B = A\overline{B} + \overline{A}B$ in Conventional CMOS. Assume a 65 nm technology. Assume that both true and inverted versions of all inputs are available to you. Note that since parts "a" and "b" can also be done independently, your mistake in "a" is not carried forward to "b".
   a. Draw the most efficient schematic
   b. Draw the most efficient stick layout diagram
   c. Estimate the area in micron square

3. <30 marks> Implement the minority function $Y = \overline{AB + C(A + B)}$ in Conventional CMOS. Assume a 65 nm technology. Note that since parts "a" and "b" can also be done independently, your mistake in "a" is not carried forward to "b".
   a. Draw the most efficient schematic
   b. Draw the most efficient stick layout diagram
   c. Estimate the area in micron square

4. <12 marks > Mark the most appropriate answer choice.
   a. The feature length in a CMOS technology refers to
      i. Minimum channel length
      ii. Minimum distance between the source and drain
      iii. Minimum width of a Poly line
      iv. All of the above
   b. In general, which side of a PMOS transistor is its source?
      i. The side connected to GND
      ii. The side connected to V_{DD}
      iii. The side with the higher potential compared to the other side
      iv. The side with a contact
   c. Which one makes a positive-edge-triggered flipflop?
      i. A high-transparent latch followed by a low-transparent latch
      ii. A low-transparent latch followed by a high-transparent latch
      iii. Two high-transparent latches
      iv. Two low-transparent latches

5. <8 marks> Indicate True or False.
   a. Body (substrate) of NMOS transistors is usually connected to the power supply. ( )
   b. P-type Silicon wafers are typically used to fabricate CMOS ICs. ( )
   c. PMOS transistors are better in transferring "0"s compared to NMOS transistors. ( )
   d. A tristate buffer produces a Z (high impedance) output when not enabled.