Assignment 4
Due ... December 2014
Maitham Shams
ELEC 4708A: Advanced Digital Integrated Circuits
Department of Electronics, Carleton University

Last Name	**First Name**	**ID**

- **Formula**

$$I_{Psat} = 4 \times 10^{-5} \frac{W}{L}(|V_{GS}| - |V_{tp}|)^{1.5}$$

$$I_{Nsat} = 1 \times 10^{-4} \frac{W}{L}(V_{GS} - V_{tn})^{1.3}$$

$$I_{sub} = I_0 \, e^{\frac{V_{GS}-V_t}{n\upsilon_T}} \left(1 - e^{\frac{-V_{DS}}{\upsilon_T}}\right), \; I_0 = \beta \upsilon_T^2 e^{1.8}, \; \upsilon_T = K\frac{T}{q}$$

$$\beta = \mu C_{ox}\frac{W}{L}, \; C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$S = n\upsilon_T \ln 10$$

$$D = \frac{CV_{DD}}{2I}, \;\; E = CV_{DD}^2$$

$$\hat{D} = NF^{\frac{1}{N}} + P, \;\; F = GBH, \;\; \hat{f} = F^{\frac{1}{N}}, \;\; H = \frac{C_{out}}{C_{in}}, \;\; \hat{N} = \log_4 F$$

$$f = gh, \;\; b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}, \;\; G = \Pi g_i, \;\; P = \Sigma p_i$$

$$\%\text{improvement} = \frac{\text{old value} - \text{new value}}{\text{old value}} \times 100$$

- **Data**

$$V_{DD} = 1 \text{ V}, \; V_{tn} = 0.30 \text{ V}, \; V_{tp} = -0.35 \text{ V}, \; L_{min} = 100 \text{ nm}, , \; t_{ox} = 20 \text{ Å}, \; n = 1.5$$

$$\mu_n = 80 \frac{\text{cm}^2}{V \cdot s}, \; \mu_p = 30 \frac{\text{cm}^2}{V \cdot s}, \; \varepsilon_{ox} = 3.9 \, \varepsilon_0, \; \varepsilon_0 = 8.85 \times 10^{-14} \frac{\text{F}}{\text{cm}}, \; d_{inv} = 10 \text{ ps}$$

I	II	III	IV	Total
/10	/6	/24	/10	/50

I. True-False Questions

$10 \times 1 = 10$ marks

Print True (T) or False (F), whichever is *more appropriate*, in the box following each statement.

1) Pseudo NMOS is a ratio-less logic style. ☐
2) Rising delay is always higher than falling delay in DCVSL. ☐
3) The out put of a PTL suffers from one V_{tp} drop. ☐
4) A flip-flop with asynchronous reset has more overhead circuitry compared to a similar flip-flop with synchronous reset. ☐
5) A low-skew inverter should be used with Domino logic gates. ☐
6) Domino logic gates do not need a foot transistor. ☐
7) Pseudo NMOS logic gates suffer from short-circuit static power dissipation when their N-net is not active. ☐
8) No matter what logic style is used, it is always more efficient to implement the inverter in the conventional CMOS style. ☐
9) Clock gating disturbs the timing restrictions of the flip-flops. ☐
10) Power gating reduces the dynamic power consumption. ☐

II. Multiple Choice Questions

$3 \times 2 = 6$ marks

Print the letter corresponding to the *most appropriate* answer in the box.

1) If the number of transistors used for implementing a function in conventional CMOS is $2n$, then how many transistors are needed to implement the same function in Pseudo NMOS style? ☐
   (a) n
   (b) $n + 1$
   (c) $n + 2$
   (d) $2n$
2) V_{OH} of an NMOS logic gate with a load resistance R and a short-circuit current I is given by .. ☐
   (a) V_{DD}.
   (b) $V_{DD} - IR$.
   (c) $VDD + IR$.
   (d) None of the above.
3) A multi-input logic gate with transistors of different sizes, has ☐
   (a) multiple g and multiple p values.
   (b) only one g and multiple p values.
   (c) multiple g but only one p values.
   (d) only one g and one p values.

III. CMOS Logic Styles

24 marks

Implement the following function in 5 different logic styles and indicate their names.

$$Y = A \oplus (B \cdot \overline{C})$$

IV. Static and Dynamic Power 10 marks

A digital system-on-chip has 5 billion transistors, of which 7% are in logic gates and the remainder in memory arrays. The average logic transistor width is 10λ and the average memory transistor width is 4λ. The logic gates have an average activity factor of 15%, while the memory activity factor is 3%. Assume that $C_{gate} = C_{diff} = 1.5$ fF/μm. Subthreshold leakage for OFF transistors is 90 nA/μm for low-V_t devices, 35 nA/μm for standard-V_t devices, and 7 nA/μm for high-V_t devices. Memory has a ratio of 1/9 of standard-V_t to low-V_t devices. The logic has a ratio of 2/3/5 of low/standard/high-V_t devices. The chip operates at 800 MHz.

A) Estimate the switching power in W.

B) Estimate the static power consumption mW.