Assignment 3
Due Friday 28 November 2014
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Last Name	**First Name**	**ID**

- **Formula**

$$I_{Psat} = 4 \times 10^{-5} \frac{W}{L}(|V_{GS}| - |V_{tp}|)^{1.5}$$

$$I_{Nsat} = 1 \times 10^{-4} \frac{W}{L}(V_{GS} - V_{tn})^{1.3}$$

$$I_{sub} = I_0 \, e^{\frac{V_{GS}-V_t}{n\upsilon_T}} \left(1 - e^{\frac{-V_{DS}}{\upsilon_T}}\right), \; I_0 = \beta \upsilon_T^2 e^{1.8}, \; \upsilon_T = K\frac{T}{q}$$

$$\beta = \mu C_{ox}\frac{W}{L}, \; C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$S = n\upsilon_T \ln 10$$

$$D = \frac{CV_{DD}}{2I}, \;\; E = CV_{DD}^2$$

$$\hat{D} = NF^{\frac{1}{N}} + P, \;\; F = GBH, \;\; \hat{f} = F^{\frac{1}{N}}, \;\; H = \frac{C_{out}}{C_{in}}, \;\; \hat{N} = \log_4 F$$

$$f = gh, \;\; b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}, \;\; G = \Pi g_i, \;\; P = \Sigma p_i$$

$$\%\text{improvement} = \frac{\text{old value} - \text{new value}}{\text{old value}} \times 100$$

- **Data**

$$V_{DD} = 1 \text{ V}, \; V_{tn} = 0.30 \text{ V}, \; V_{tp} = -0.35 \text{ V}, \; L_{min} = 100 \text{ nm}, , \; t_{ox} = 20 \text{ Å}, \; n = 1.5$$

$$\mu_n = 80 \frac{\text{cm}^2}{V \cdot s}, \; \mu_p = 30 \frac{\text{cm}^2}{V \cdot s}, \; \varepsilon_{ox} = 3.9 \, \varepsilon_0, \; \varepsilon_0 = 8.85 \times 10^{-14} \frac{\text{F}}{\text{cm}}, \; d_{inv} = 10 \text{ ps}$$

I	II	III	IV	Total
/10	/10	/5	/35	/60

I. True-False Questions

$10 \times 1 = 10$ marks

Print True (T) or False (F), whichever is *more appropriate*, in the box following each statement.

1) During the discharge of an output node (in a logic gate) the energy stored in its capacitance is dumped into ground . ..... ☐
2) Logical effort g is independent of the size of the transistors in a logic gate. ..... ☐
3) Gate leakage of PMOS transistors is lower than NMOS transistors of the same t_{ox}. ..... ☐
4) The larger the transistors in the critical path of a circuit, the lower the delay. ..... ☐
5) The dynamic power dissipation of a NAND gate whose one input is grounded, equals zero. ... ☐
6) Method of Logical Effort is used to optimize the power dissipation in a digital CMOS circuit. . ☐
7) High V_t transistors can be used in non-critical paths to save energy. ..... ☐
8) Instantaneous power is used to determine the wire thickness . ..... ☐
9) A digital circuit sized for minimum delay, has the maximum power consumption. ..... ☐
10) The ratio of the stored energy at the output capacitance of an inverter to the heat dissipated by its PMOS transistor is 1. ..... ☐

II. Multiple Choice Questions

$5 \times 2 = 10$ marks

Print the letter corresponding to the *most appropriate* answer in the box.

1) If the optimum number of inverters driving a load is 5, and the input capacitance of the first inverter is 3 units, what is the input capacitance of the last inverter? ..... ☐
   (a) 15
   (b) 768
   (c) 48
   (d) 1875
2) If we ignore the parasitic delay of inverters, the optimum stage effort is ..... ☐
   (a) 4.
   (b) π.
   (c) e.
   (d) 2.
3) Short-circuit power dissipation is typically about ..... of the total dynamic power? ..... ☐
   (a) 10%
   (b) 30%
   (c) 50%
   (d) 70%

4) Decreasing which parameter among the following is most effective in reducing dynamic power dissipation? ..... ☐

   (a) Frequency
   (b) Switching activity
   (c) Power supply voltage
   (d) Effective capacitance

5) If all transistor sizes are the same, and if all inputs are low (i.e. 0), which of the following logic gates has the highest static energy dissipation? ..... ☐

   (a) Inverter
   (b) NAND
   (c) NOR
   (d) Tristate inverter

III. Logical Effort

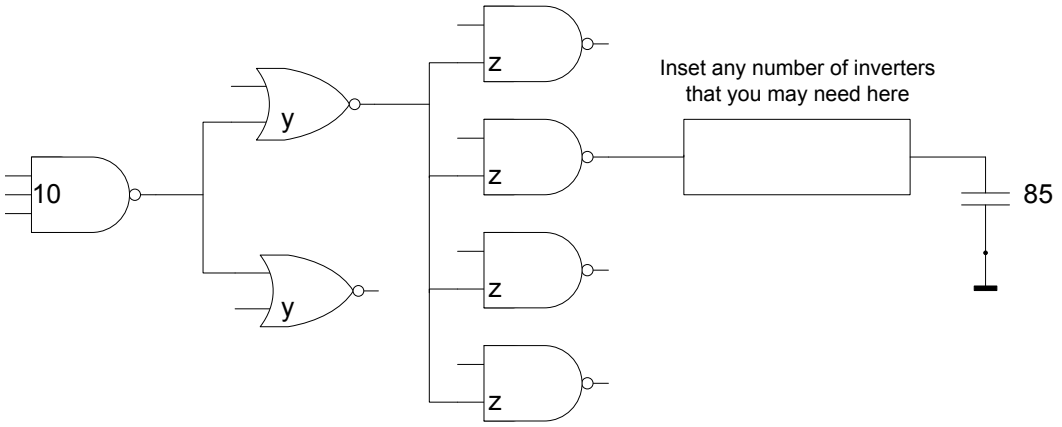
5 marks

For the conventional CMOS logic gate implementing $Z = (A + B\bar{C})(E + \bar{F})$ find p and g for different inputs.

IV. Delay Optimization

35 marks

Consider the following circuit. The input NAND has an input capacitance of 10 units. The output capacitance is equivalent to 85 units. The units can be considered W/L of a transistor with minimum width and length. Assume that the polarity of the output is not important.



A) Beside each logic gate indicate p, g, b, and h. 6

B) Calculate the path effort F for the critical path in the circuit. 2

C) Find the optimum number of stages $\hat{N}$ for minimizing the delay in the circuit. Modify the circuit, if necessary to achieve the minimum delay. Revise the parameters p, g, b, and h for the logic gates and include inserted inverters. 5

D) Calculate the minimum possible *normalized* and *absolute* delays for the circuit. 3

E) Find the unknown input capacitances for the logic gates, including any inserted inverters. [6]

F) Draw a schematic diagram of the logic gates in the modified circuit indicating the actual W/L of all transistors. [3]

G) If you inserted any inverters, calculate how much you improved the delay by doing so? Use the formula on the front page for % improvement. [5]

H) Calculate how much you saved or wasted area (or energy dissipation) by doing so. You may take the total transistor widths as an indication for the area (and energy)? [5]