Assignment 2, Fall 2014
Due Wedensday 22 October 2014

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# ELEC 4708A: Advanced Digital Integrated Circuits

Department of Electronics, Carleton University

| **Last Name** | **First Name** | **ID** |
|---|---|---|
| | | |

- **Formula**

$$I_{Psat} = 4 \times 10^{-5} \frac{W}{L}(|V_{GS}| - |V_{tp}|)^{1.5}$$

$$I_{Nsat} = 1 \times 10^{-4} \frac{W}{L}(V_{GS} - V_{tn})^{1.3}$$

$$I_{sub} = I_0 \, e^{\frac{V_{GS}-V_t}{n\upsilon_T}} \left(1 - e^{\frac{-V_{DS}}{\upsilon_T}}\right), \; I_0 = \beta \upsilon_T^2 e^{1.8}, \; \upsilon_T = K\frac{T}{q}$$

$$\beta = \mu C_{ox}\frac{W}{L}, \; C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$S = n\upsilon_T \ln 10$$

- **Data**

$$V_{DD} = 1 \text{ V}, \; V_{tn} = 0.30 \text{ V}, \; V_{tp} = -0.35 \text{ V}, \; L_{\text{min}} = 100 \text{ nm}, , \; t_{ox} = 20 \; \mathring{A}, \; n = 1.5$$

$$\mu_n = 80 \, \frac{\text{cm}^2}{V \cdot s}, \; \mu_p = 30 \, \frac{\text{cm}^2}{V \cdot s}, \; \varepsilon_{ox} = 3.9 \, \varepsilon_0, \; \varepsilon_0 = 8.85 \times 10^{-14} \, \frac{\text{F}}{\text{cm}}$$

| Q1 | Q2 | Q3 | Q4 | Q5 | Total |
|---|---|---|---|---|---|
| /10 | /20 | /10 | /10 | /10 | /70 |

## [1] Multiple Choice Questions

$5 \times 2 = 10$ marks

Circle the *most appropriate* answer.

A) What happens to the superthreshold current (i.e. ON current, or operation current) and subthreshold current (i.e. OFF current, or leakage current) in CMOS circuits as the temperature rises?

(a) Superthreshold and subthreshold currents both increase.

(b) Superthreshold current increases, while subthreshold current decreases.

(c) Superthreshold and subthreshold currents both decrease.

(d) Superthreshold current decreases, while subthreshold current increases.

B) The gate tunneling current, as a function of the gate-oxide thickness,

(a) increases linearly.

(b) increases exponentially.

(c) decreases linearly.

(d) decreases exponentially.

C) Compare the speed of similarly-sized PMOS and NMOS transistors in a CMOS technology under the same environmental conditions.

(a) NMOS transistor is about 3 times faster.

(b) PMOS transistor is about 2 times faster.

(c) They have the same speed.

(d) Depends on temperature.

D) For current CMOS technologies, the main contributer to the static power dissipation is

(a) Gate tunneling leakage.

(b) Subthreshold leakage.

(c) Junction leakage.

(d) Gate induced drain leakage.

E) What should be the variations considered for $L$, $V_t$, and $t_{ox}$, respectively, for the fast (F) corner simulations?

(a) Long, high, thin.

(b) Short, low, thin.

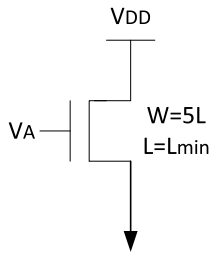
(c) Long, low, thick.

(d) Short, high, thick.

## [2] MOSFET capacitance and current

20 marks

Consider the depicted NMOS transistor and calculate the following parameters. Marks will be deducted for results without appropriate units. Assume that the thermal voltage $\upsilon_T = 26$ mV at 300 K (i.e. 27 °C, considered room temperature). *Note: make sure you know how to use the formula if it was a PMOS transistor.*




A) $C_{ox}$ in fF/$\mu m^2$ and the total gate-oxide capacitance in fF. 2

B) $\beta$ in A/V$^2$. 2

C) $I_{ON}$, i.e. $V_A = V_{DD}$, in $\mu$A. 2

D) $I_{OFF}$, i.e. $V_A = 0$, at room temperature in nA. 2

E) $I_{OFF}$, at 75 °C in nA. Assume you do not know the value of $q$. 2

F) $I_d$ when the transistor is barely ON, i.e. $V_{GS} = V_t$? 2

G) $I_d$ when $V_{GS} = V_{DD}/2$? 2

H) The subthreshold slope? 2

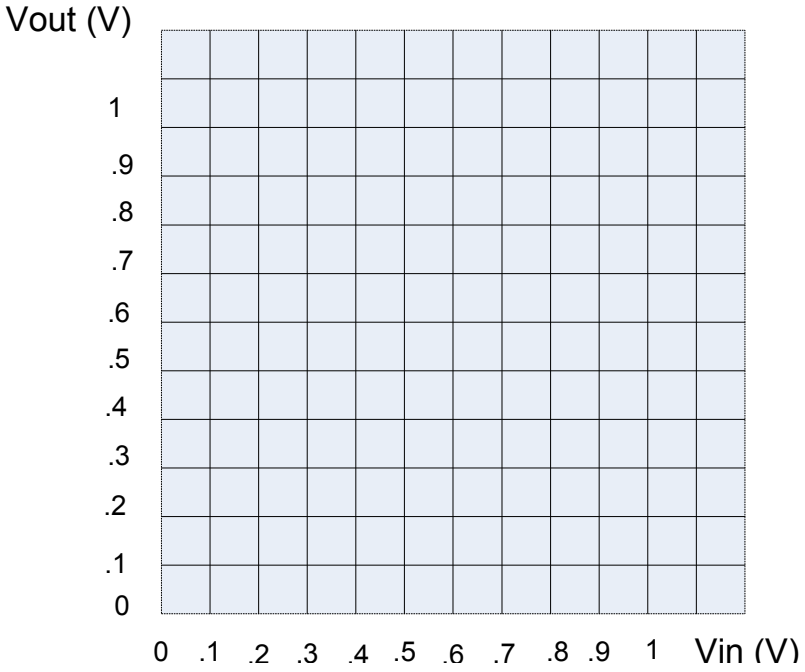
I) Gate potential when the current is 1000 times larges than the OFF current? 2

J) Size (i.e. wisth) ratio of PMOS to NMOS transistor for equal ON current? 2

## [3] VTC

10 marks

A novel inveter has $V_{IL} = 0.3\ V$, $V_{IH} = 0.6\ V$, $V_{OL} = 0.1\ V$, and $V_{OH} = 0.9\ V$. Assume $V_{DD} = 1\ V$.

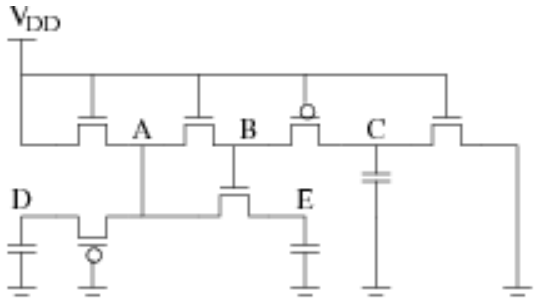



- **3.a)** Plot the VTC (output voltage versus input voltage) of this inverter and obtain values of noise margins high and low: $NM_H =$ ....., and $NM_L =$ ..... .
- **3.b)** Plot the VTC of an ideal inverter on the same graph and obtain values of $V_{IL} =$ .....$V$, $V_{IH} =$ .....$V$, $V_{OL} =$ .....$V$, $V_{OH} =$ .....$V$, $NM_H =$ ....., and $NM_L =$ ..... No partial marks!

## [4] Pass Transistors

10 marks

Obtain the steady-state voltages at the nodes of the following circuit. All capacitances are 0.1 pF each, all transistors have $W/L = 3$, $V_{DD} = 1$ v, $V_{tn} = 0.25$ v, $V_{tp} = -0.35$ v, $andL = 100$ nm. No partial marks!




- $V_A =$ ....., $V_B =$ ....., $V_C =$ ....., $V_D =$ ....., $V_E =$ .....

## [5] Leakage

10 marks

Find the subthreshold current for a NAND gate built from unit transistors, i.e. $(W/L)_p = 4$, $(W/L)_n = 2$. Assume inputs A=B=0. Show that the subthreshold current through the series transistors is half that of an inverter if $n = 1$.