Multistage and Power Amplifiers

- Compared to single stage amplifier, multistage amplifiers provide increased input resistance, reduced output resistance, increased gain, and increased power handling capability
- Multistage amplifiers commonly implemented on integrated circuits where large numbers of transistors with common (matched) parameters are available
- Typical inverter (Common Emitter) has moderately large gain and has input and output resistances in the Kilohm range
- Follower configuration has much higher input resistance, lower output resistance but has only unity gain
- Amplifier requires the desirable features of both configurations

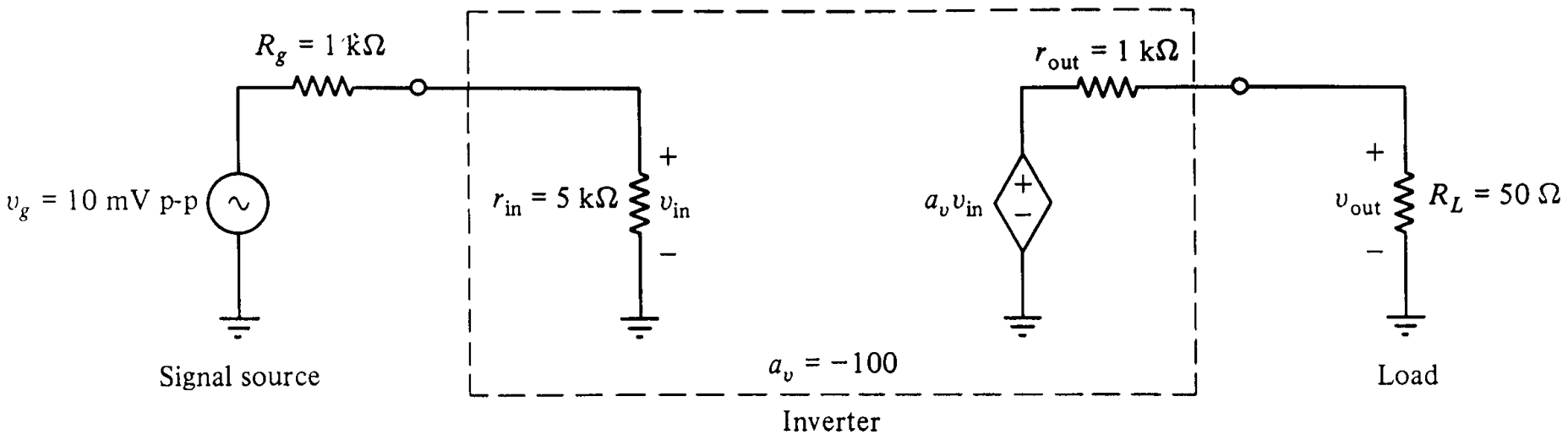


Figure 12.1 Linear model of a single-stage inverter connected to signal source and load.

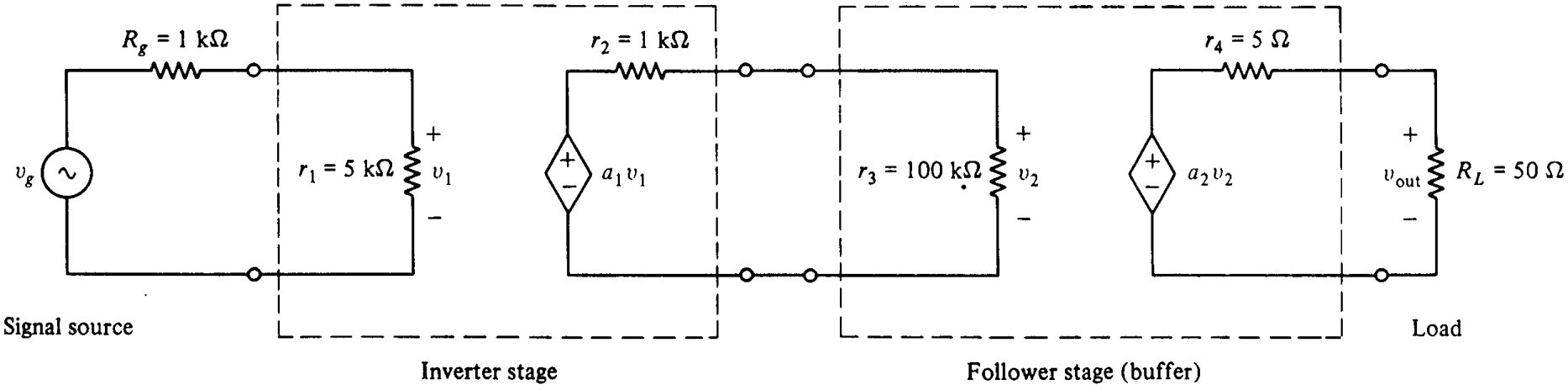
$$v_{IN} = v_g \frac{r_{IN}}{r_{IN} + R_g} = 0.83 v_g$$

$$v_{OUT} = a_v \, v_{IN} \frac{R_L}{R_L + r_{OUT}} \cong -4.0 v_g$$

Two Port Amplifier Cascade

- Impact of input and output loading can be minimized by cascading two amplifiers

Figure 12.2 Cascaded amplifier consisting of inverter stage and follower stage.

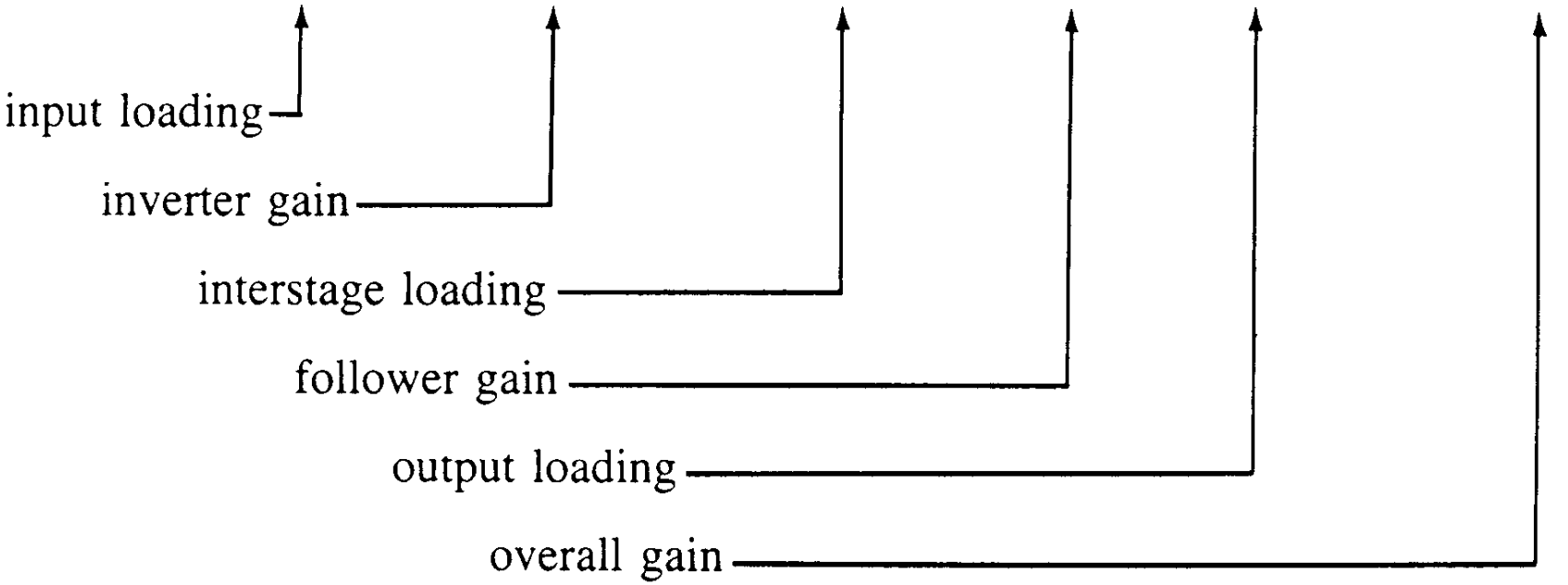


$$
\begin{aligned}
v_{\text{out}} &= (a_2 v_2)\,\frac{R_L}{R_L + r_4} \\
&= (a_1 v_1)\,\frac{r_3}{r_3 + r_2}\; a_2\,\frac{R_L}{R_L + r_4} \\
&= v_g\,\frac{r_1}{r_1 + R_g}\;\frac{a_1 r_3}{r_3 + r_2}\;\frac{a_2 R_{\text{L}}}{R_{\text{L}} + r_4}
\end{aligned}
\tag{12.5}
$$

For these values, the overall cascade gain (12.5) becomes

$$\frac{v_{\text{out}}}{v_g} = \left(\frac{5\ \text{k}\Omega}{5\ \text{k}\Omega + 1\ \text{k}\Omega}\right)(-100)\left(\frac{100\ \text{k}\Omega}{100\ \text{k}\Omega + 1\ \text{k}\Omega}\right)(1)\left(\frac{50\ \Omega}{50\ \Omega + 5\ \Omega}\right) \tag{12.7}$$

$$= \quad (0.83) \quad (-100) \quad (0.99) \quad (1) \quad (0.91) \quad \simeq -75$$



- Multistage cascading is used to create amplifiers with high input resistance, low output resistance and large gains

Multistage Amplifier Biasing

- It is possible to create multistage cascade where each stage is separately biased and coupled to adjacent stages via DC blocking capacitors

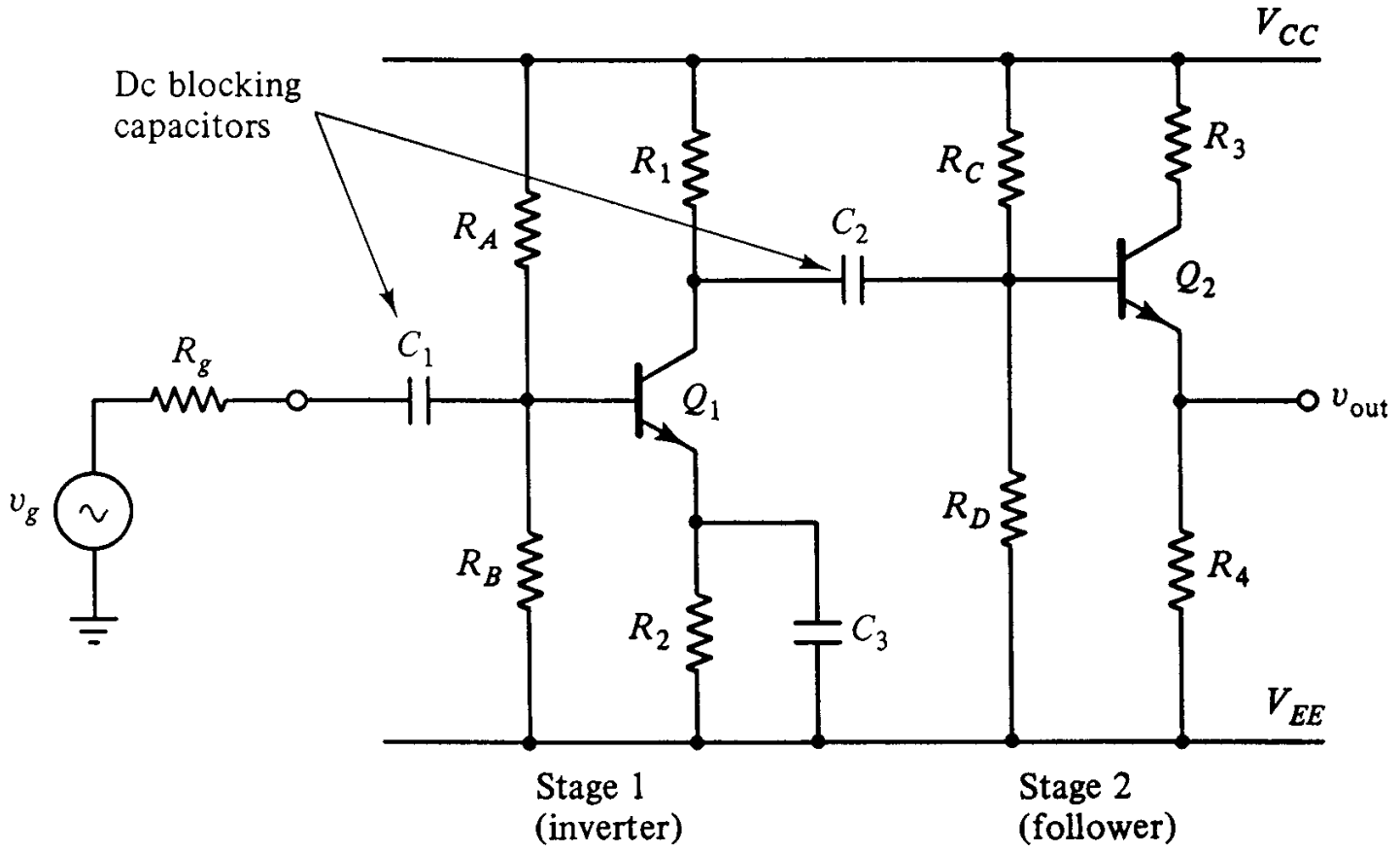


Figure 12.3
Possible implementation of the two-stage inverter-follower cascade. This design technique is not optimal because it uses many discrete capacitors.

- Amplifier gain is reduced at low frequencies
- Difficult to build integrated circuits with large value blocking capacitors
- DC coupled amplifier

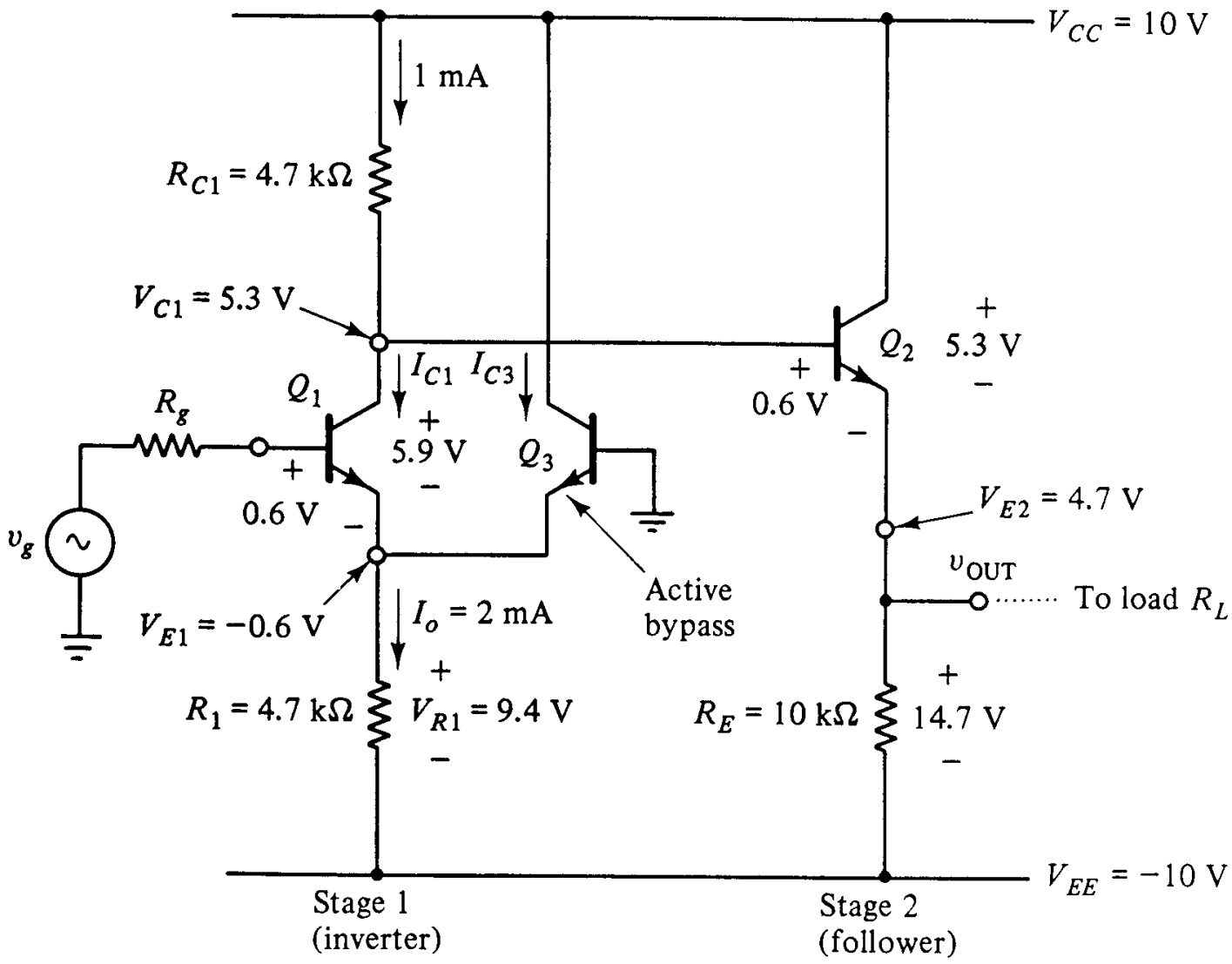


Figure 12.4
Two-stage dc-coupled cascaded amplifier.

Small Signal Model of Cascaded Amplifer

Inverter

If R >> R_{TH} Looking into the emitter of Q_3

$$r_{IN1} = r_{\pi 1} + r_{\pi 3} = 2r_{\pi 1}$$

$$r_{OUT1} = R_{C1}$$

$$a_1 = \frac{-\beta_{o1} R_{C1}}{r_{\pi 1} + r_{\pi 3}} = \frac{-g_{m1} R_{C1}}{2}$$ (Midband Gain)

- Assuming matched devices and r_o of Q_1, Q_2 and Q_3 is large enough to be ignored

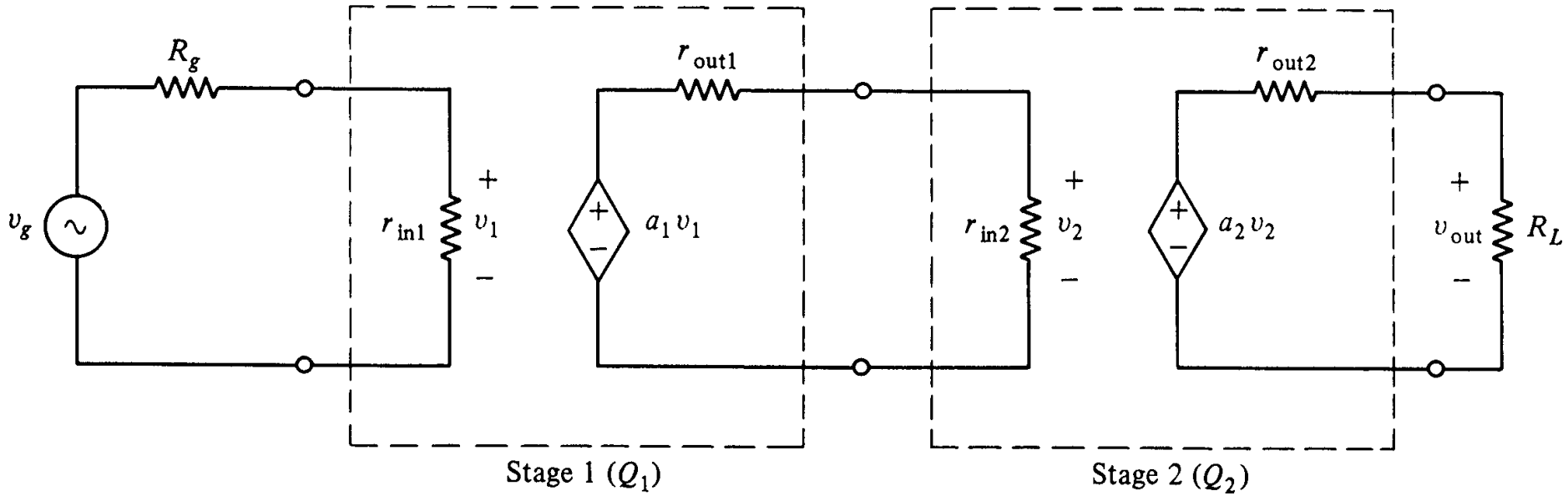
Follower (Stage 2)

$$r_{IN2} = r_{\pi 2} + (\beta_{o2} + 1) R_E$$ (Without R_L Connected)

$$r_{OUT2} = R_E \left\| \frac{r_{OUT1} + r_{\pi 2}}{\beta_{o2} + 1} \right.$$

$$a_2 = \frac{(\beta_{o2} + 1) R_E}{r_{\pi 2} + (\beta_{o2} + 1) R_E}$$

Figure 12.5 Equivalent cascade model of the amplifier of Fig. 12.4.



$$\frac{v_{\text{out}}}{v_g} = a_1 a_2 \frac{r_{\text{in1}}}{R_g + r_{\text{in1}}} \frac{r_{\text{in2}}}{r_{\text{out1}} + r_{\text{in2}}} \frac{R_L}{R_L + r_{\text{out2}}} \tag{12.21}$$

Substituting the expressions (12.15) through (12.20) into this equation yields

$$\frac{v_{\text{out}}}{v_g} = \frac{-\beta_{o1} R_{C1}}{r_{\pi 1} + r_{\pi 3}} \times \frac{(\beta_{o2} + 1) R_E}{r_{\pi 2} + (\beta_{o2} + 1) R_E} \times \frac{r_{\pi 1} + r_{\pi 3}}{R_g + r_{\pi 1} + r_{\pi 3}}$$

stage 1 gain — stage 2 gain — input loading factor

$$\times \frac{r_{\pi 2} + (\beta_{o2} + 1) R_E}{R_{C1} + r_{\pi 2} + (\beta_{o2} + 1) R_E} \times \frac{R_L}{R_L + r_{\text{out2}}} \tag{12.22}$$

interstage loading factor — output loading factor

Cancellation of factors in numerator and denominator in Eq. (12.22) leads to

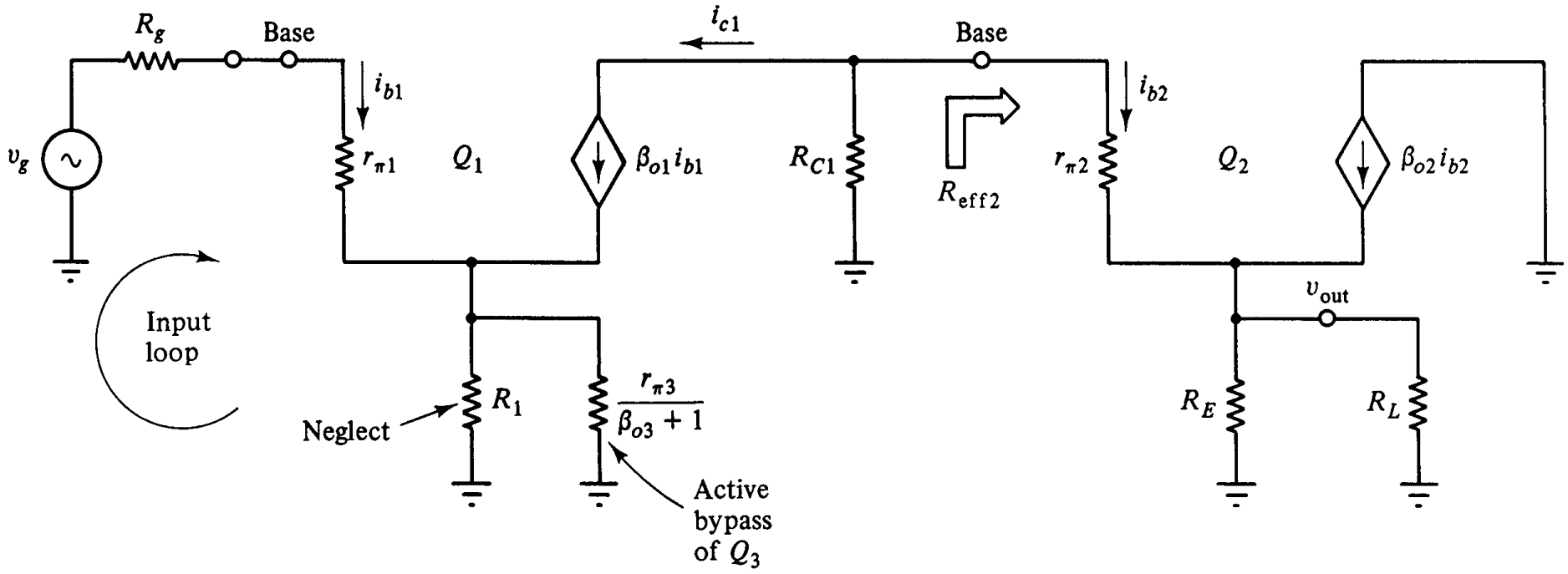
$$\frac{v_{\text{out}}}{v_g} = \frac{-\beta_{o1} R_{C1} (\beta_{o2} + 1) R_E}{(R_g + r_{\pi 1} + r_{\pi 3})[R_{C1} + r_{\pi 2} + (\beta_{o2} + 1) R_E]} \frac{R_L}{R_L + r_{\text{out2}}} \tag{12.23}$$

- Including this factor in the gain expression (12.23) yields the overall amplifier gain when the load resistor R_L is connected:

$$\frac{v_{\text{out}}}{v_g} = \frac{-\beta_{o1} R_{C1} (\beta_{o2} + 1)(R_E \parallel R_L)}{(R_g + r_{\pi 1} + r_{\pi 3})[R_{C1} + r_{\pi 2} + (\beta_{o2} + 1)(R_E \parallel R_L)]} \qquad \textbf{(12.26)}$$

- The amplifier gain can also be derived from the complete small signal model

Figure 12.6 Complete small-signal model for the circuit of Fig. 12.4.



Example:

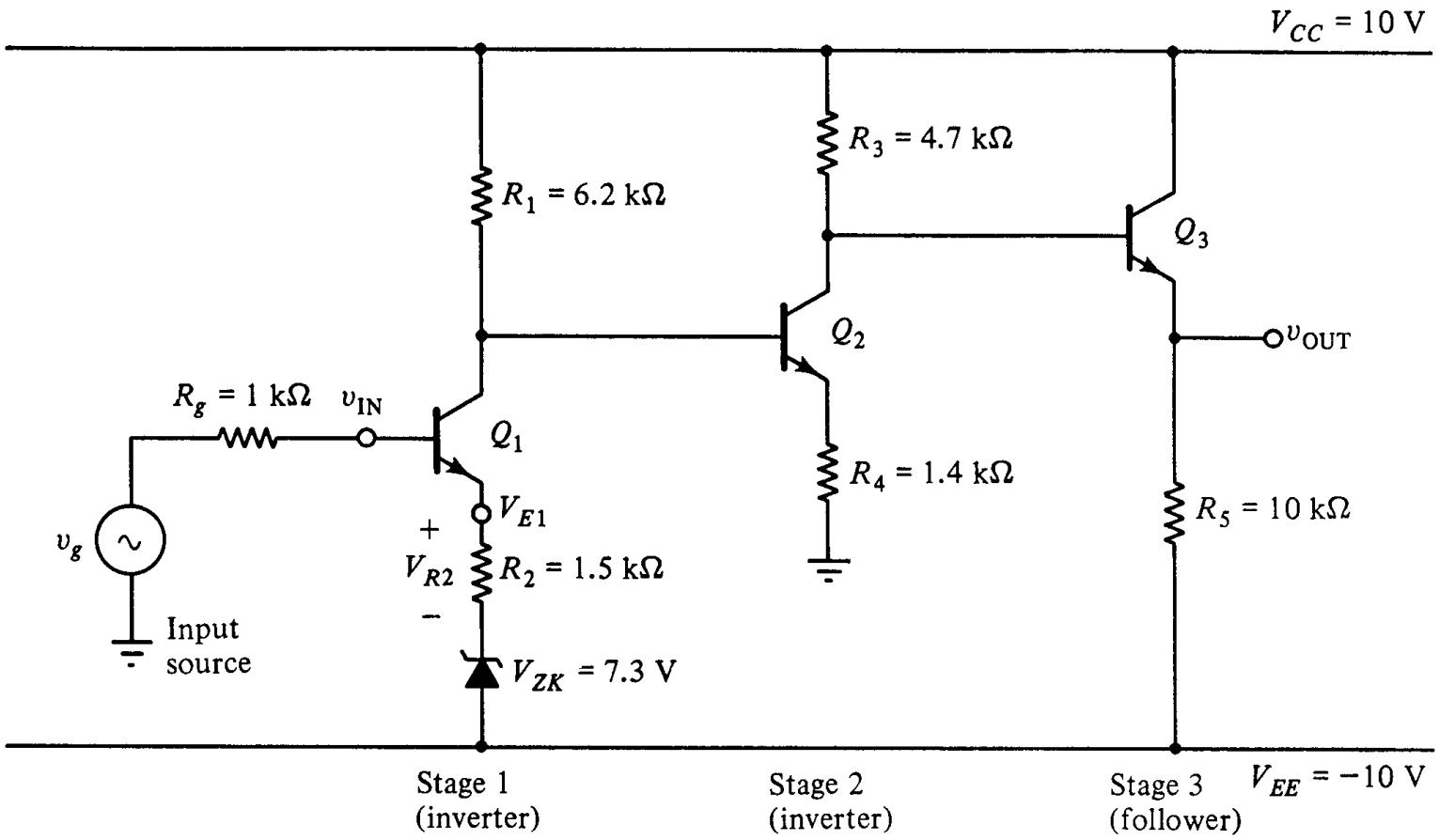


Figure 12.7
Three-stage dc-coupled cascaded amplifier.

TABLE 12.1 Gain and Resistance Parameters of the Cascade of Fig. 12.7

Parameter	Stage 1	Stage 2	Stage 3
a_v	$\dfrac{-\beta_{o1}R_1}{r_{\pi 1} + (\beta_{o1} + 1)R_2} \simeq \dfrac{-R_1}{R_2}$	$\dfrac{-\beta_{o2}R_3}{r_{\pi 2} + (\beta_{o2} + 1)R_4} \simeq \dfrac{-R_3}{R_4}$	$\dfrac{(\beta_{o3} + 1)R_5}{r_{\pi 3} + (\beta_{o3} + 1)R_5} \simeq 1$
r_{in}	$r_{\pi 1} + (\beta_{o1} + 1)R_2 \simeq \beta_{o1}R_2$	$r_{\pi 2} + (\beta_{o2} + 1)R_4 \simeq \beta_{o2}R_4$	$r_{\pi 3} + (\beta_{o3} + 1)R_5 \simeq \beta_{o3}R_5$
r_{out}	R_1	R_3	$R_5 \left\| \dfrac{r_{\pi 3} + R_3}{\beta_{o3} + 1} \right.$

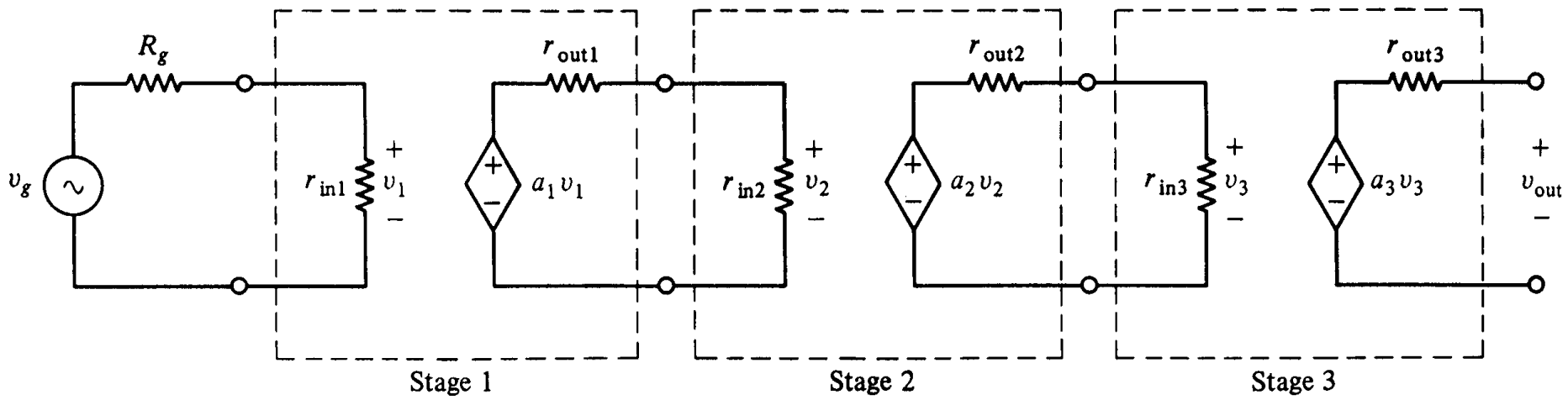


Figure 12.8 Two-port cascade of the amplifier of Fig. 12.7.

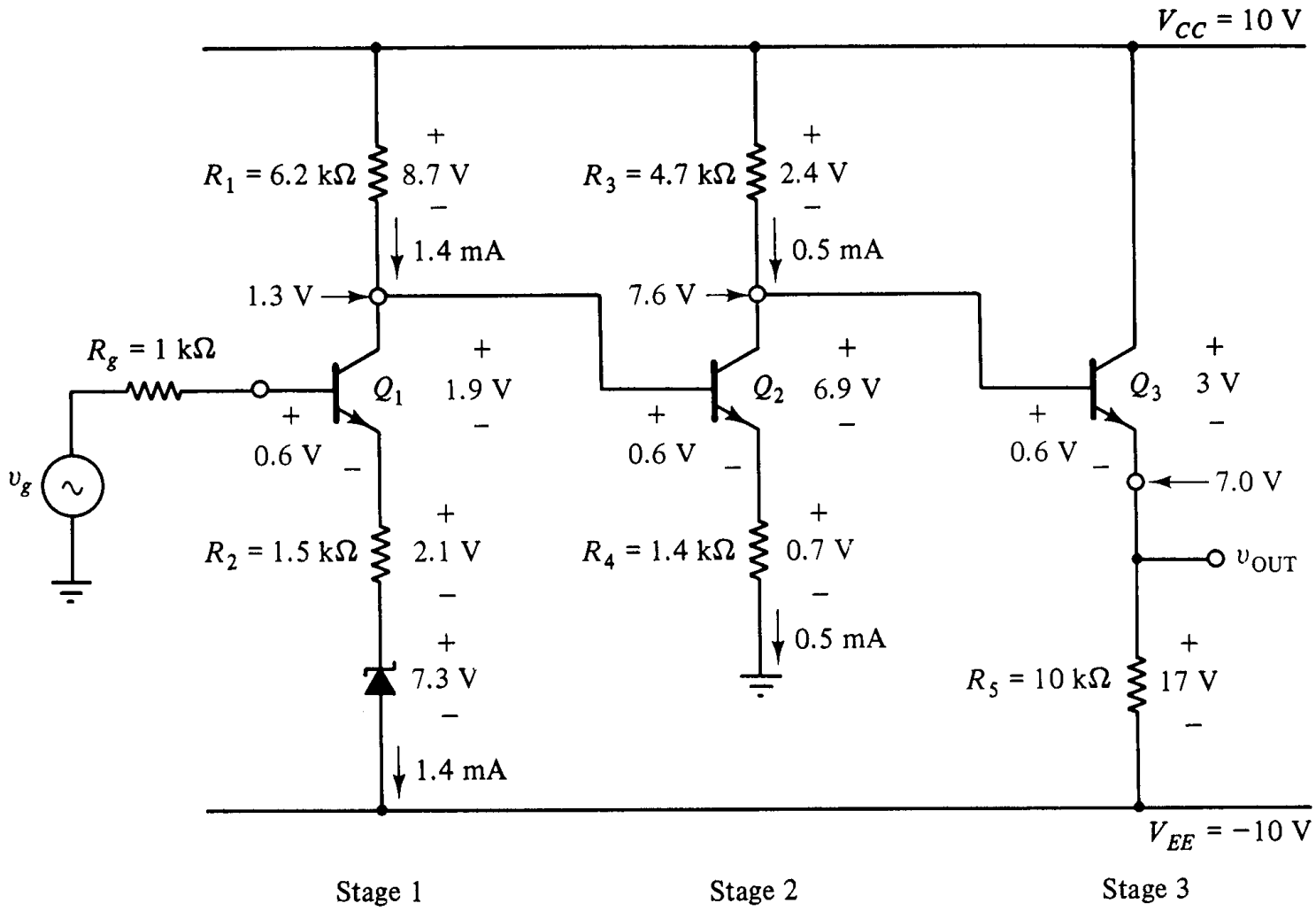
$$\frac{v_{out}}{v_g} = (a_1)\ (a_2)\ (a_3)\ \frac{r_{in1}}{R_g + r_{in1}}\ \frac{r_{in2}}{r_{in2} + r_{out1}}\ \frac{r_{in3}}{r_{in3} + r_{out2}}$$

$$\simeq \frac{-R_1}{R_2}\ \frac{-R_3}{R_4}(1)\ \frac{\beta_{o1}R_2}{R_g + \beta_{o1}R_2}\ \frac{\beta_{o2}R_4}{R_1 + \beta_{o2}R_4}\ \frac{\beta_{o3}R_5}{R_3 + \beta_{o3}R_5} \qquad \textbf{(12.36)}$$

DC Level Shifting

- In DC - coupled multistage cascade the output bias level of each stage increases to maintain the collector more positive than the base (constant current operation)
- If this voltage “stacking” is severe, little swing room is left in the final stages of the cascade

Figure 12.9
Multistage cascade of Fig. 12.7 with dc bias voltages indicated.



- Voltage stacking can be alleviated by the use of DC level shifting
- Level shifting alters the bias distribution but not the gain
- Simple method involves the insertion of a passive device with a constant DC voltage drop

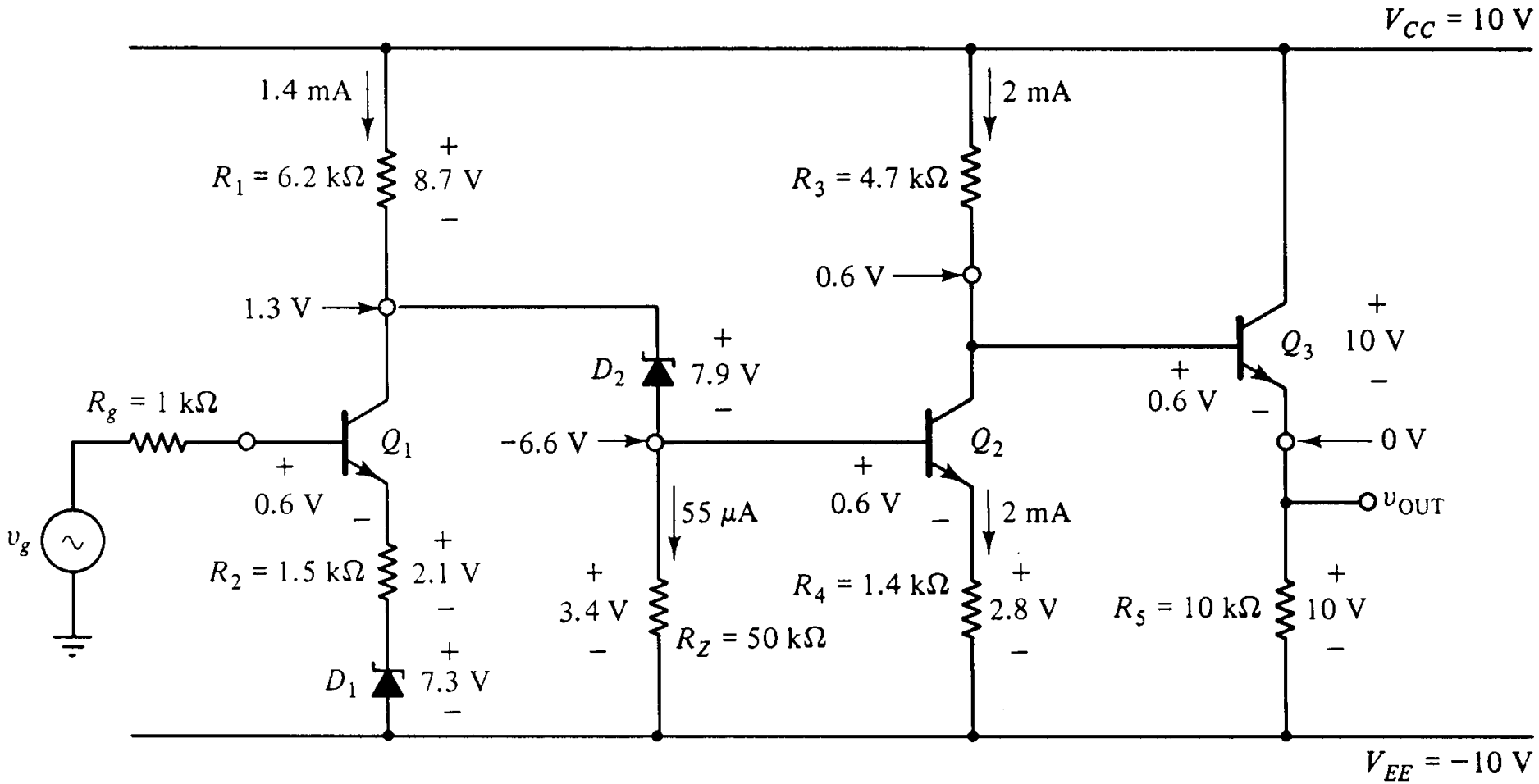


Figure 12.10 Zener diode level shifter added to the circuit of Fig. 12.9. BJT base currents are neglected in computing the indicated bias levels.

- By using complementary devices, active level shifting can be combined with amplification

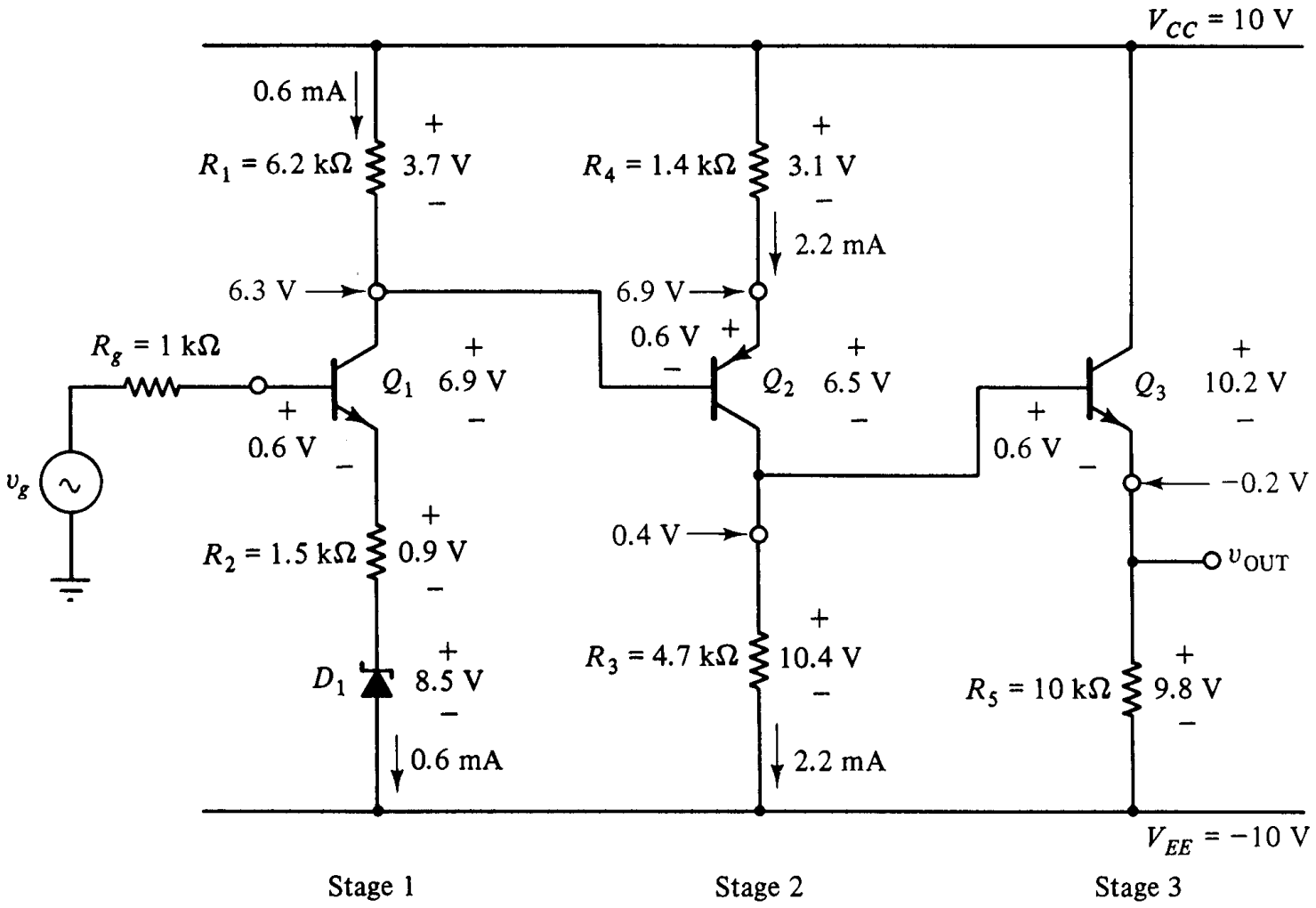


Figure 12.11
PNP level shifter incorporated into the circuit of Fig. 12.9. BJT base currents are neglected in computing the indicated bias levels.

- In MOSFET circuits, DC level shifting is implemented using complementary NMOS and PMOS devices

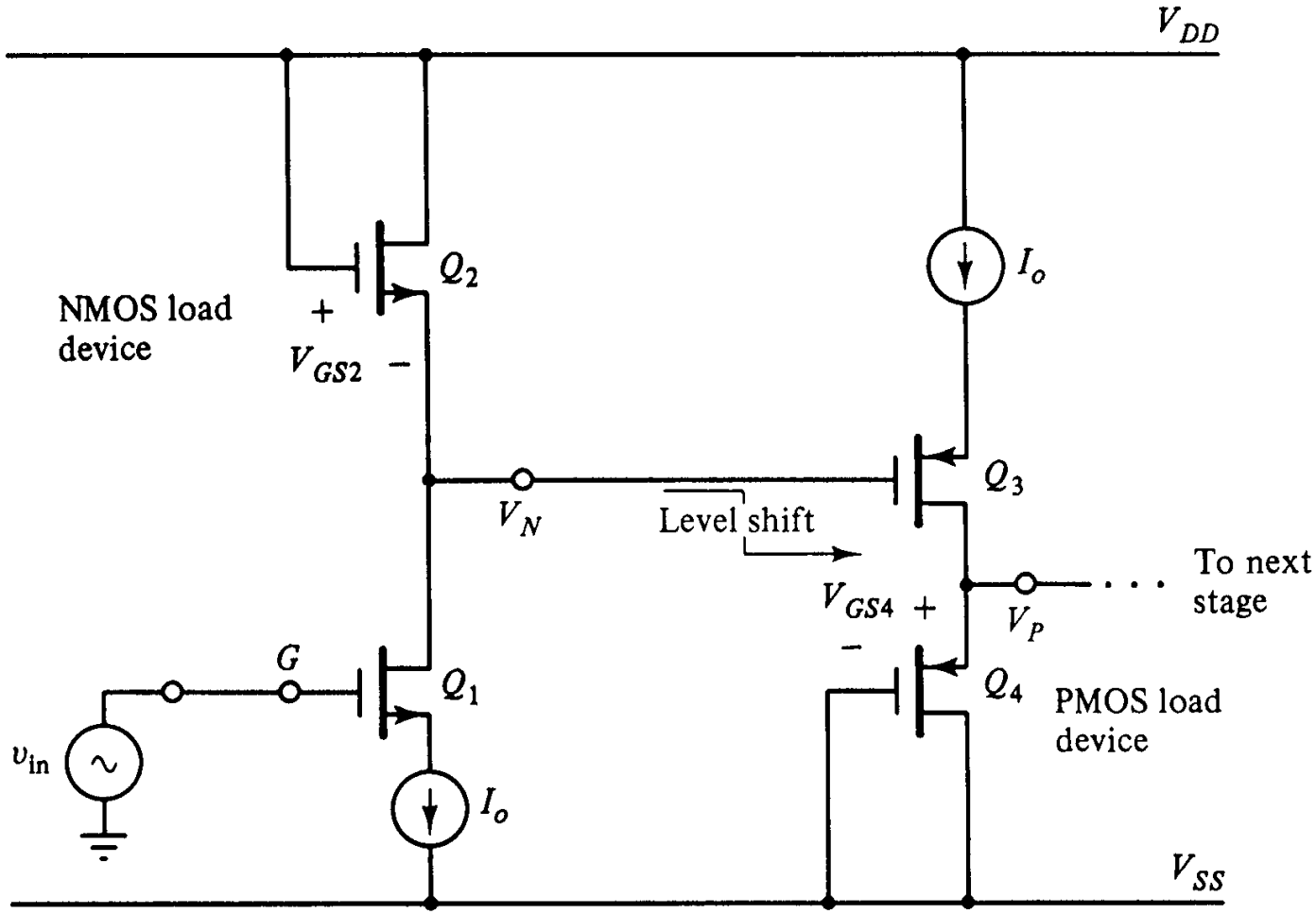
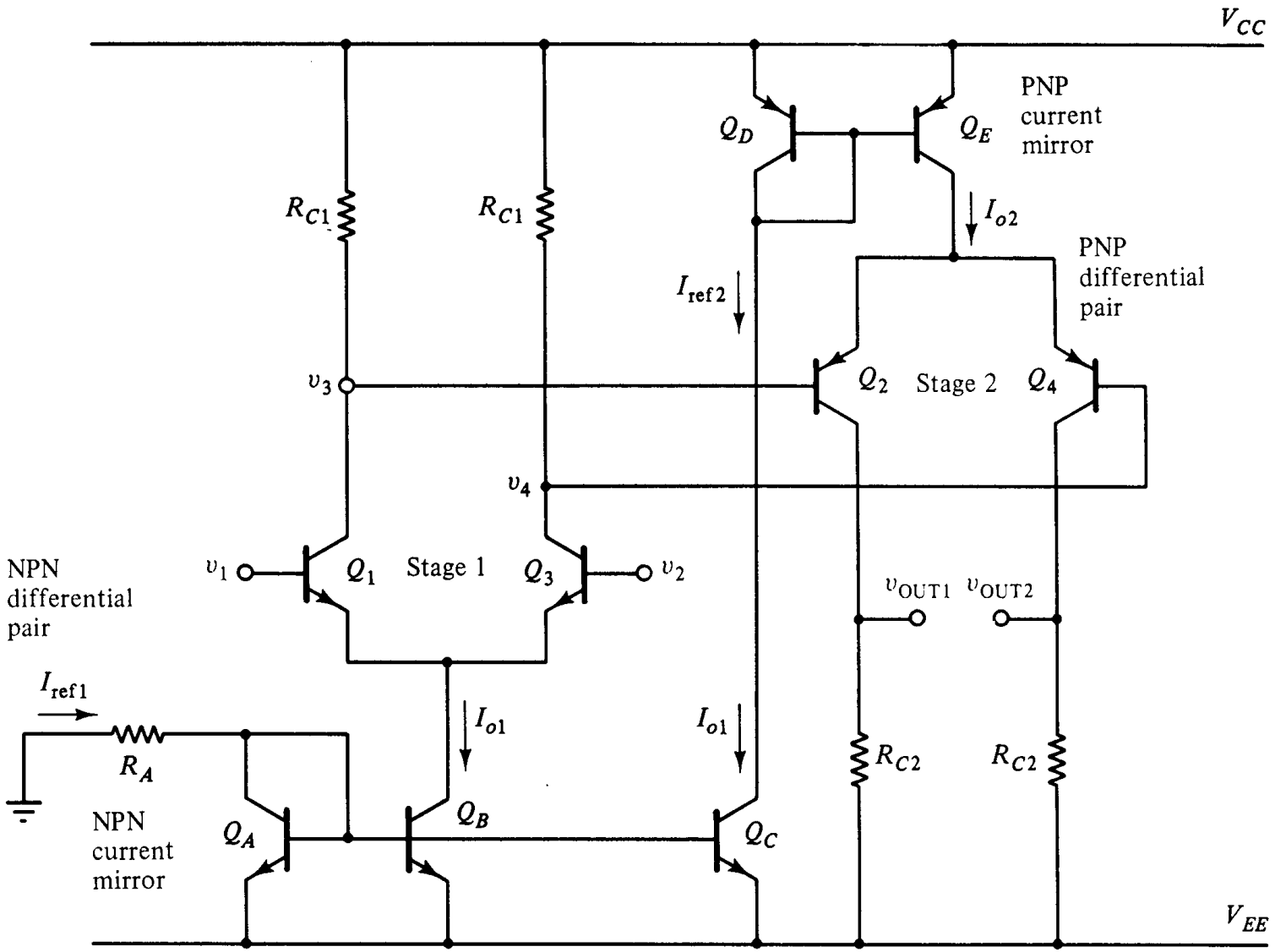


Figure 12.12 Complementary *n*-channel and *p*-channel MOSFET multistage amplifier cascade.

Differential Cascade

Figure 12.13
Two-stage BJT differential amplifier cascade with complementary NPN and PNP devices.



Power Amplification Stages

- In many designs an amplifier is required to deliver large amounts of power to a passive load. The power may be a large current to a small resistance or a large voltage to a moderate resistance (impedance)
- Using a linear amplifier the power wasted in the active device is comparable to the power delivered to the load. Devices in the output stage must be capable of dissipating this excess power
- Alternative configurations offer increased efficiency at the expense of true linear operation

Complementary Pair (Class B) Output

- When an amplifier is required to deliver large load currents it is desirable to bias the voltage of its output terminal near ground. This minimizes the bias power dissipated in both the load element and the active devices of the output stage

Figure 12.17
Complementary-pair "push-pull" amplifier output stage made from BJTs. This circuit is a class B amplifier since neither device is biased in its active region.

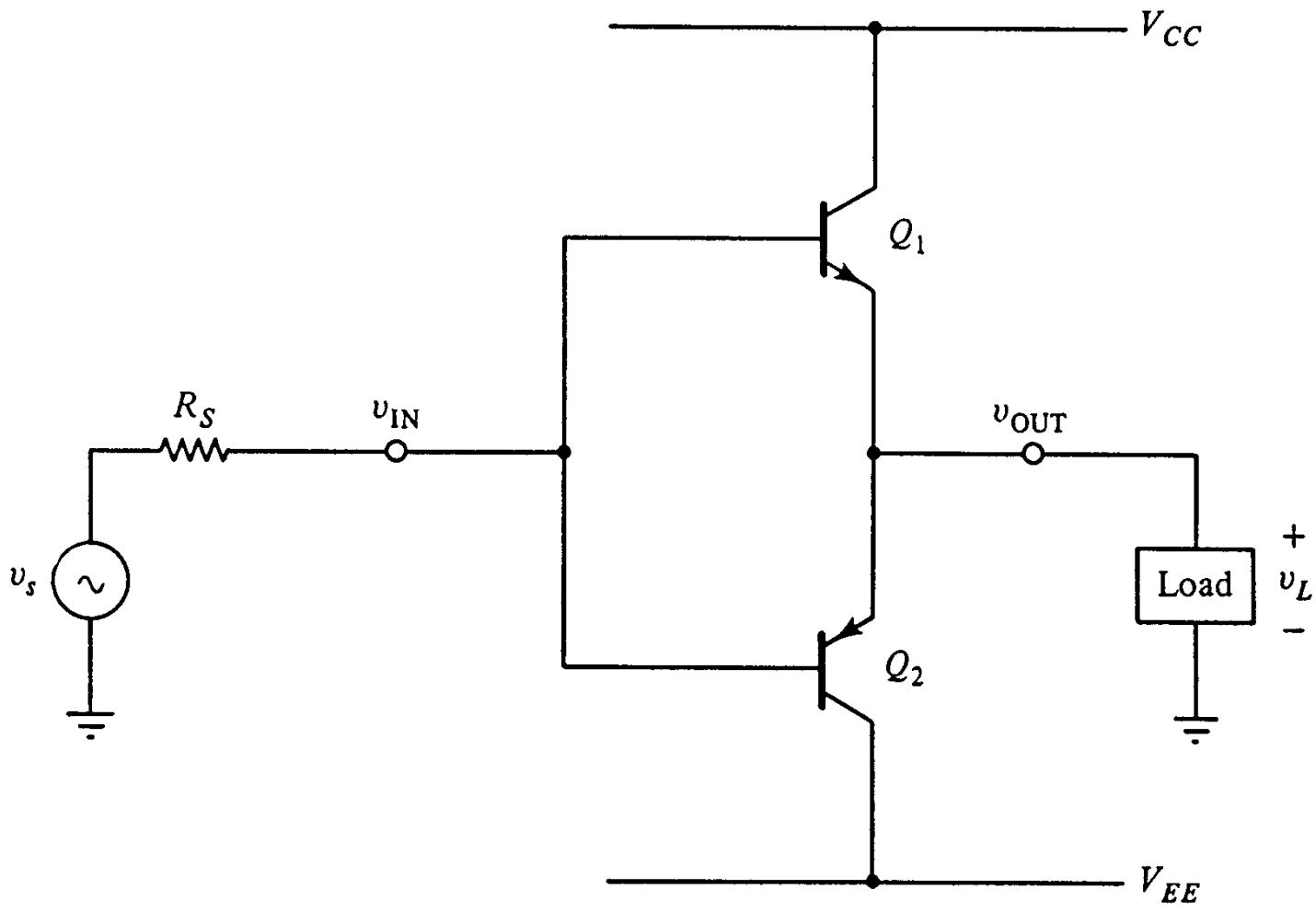
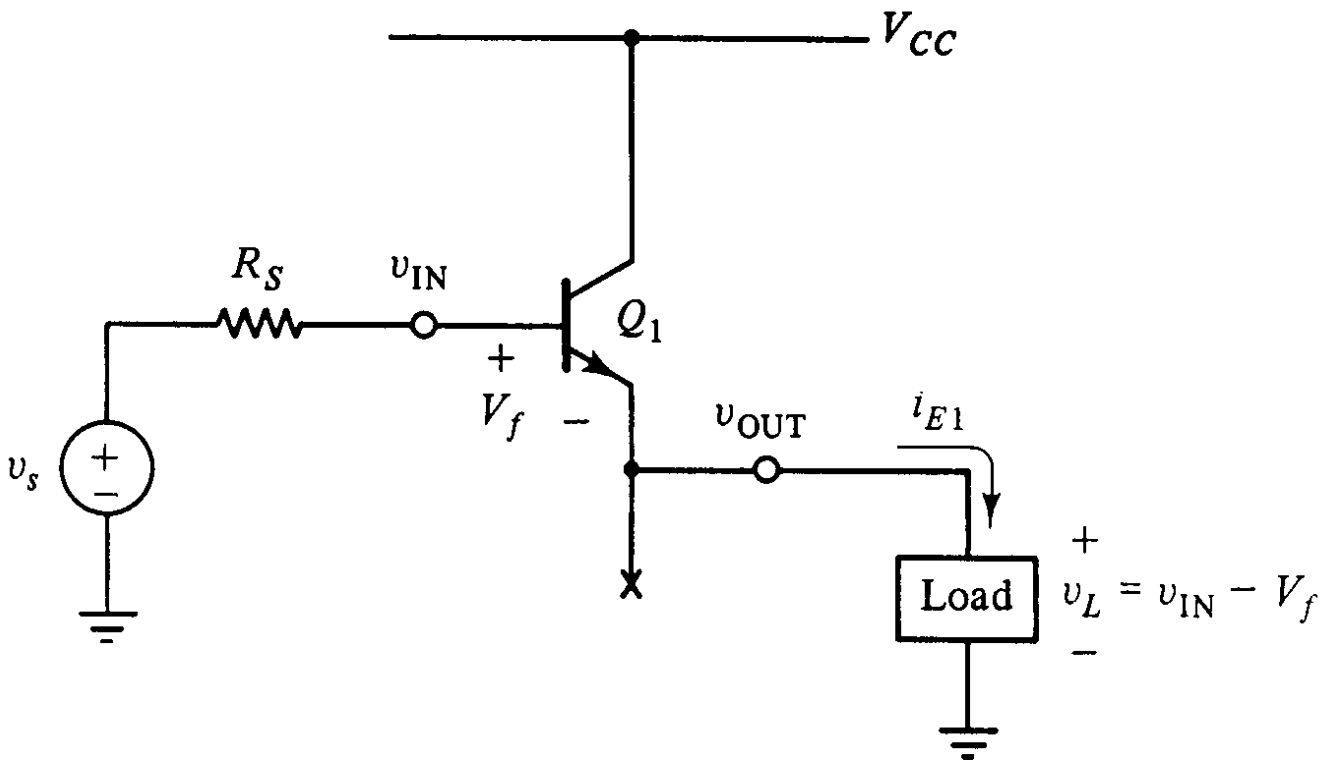
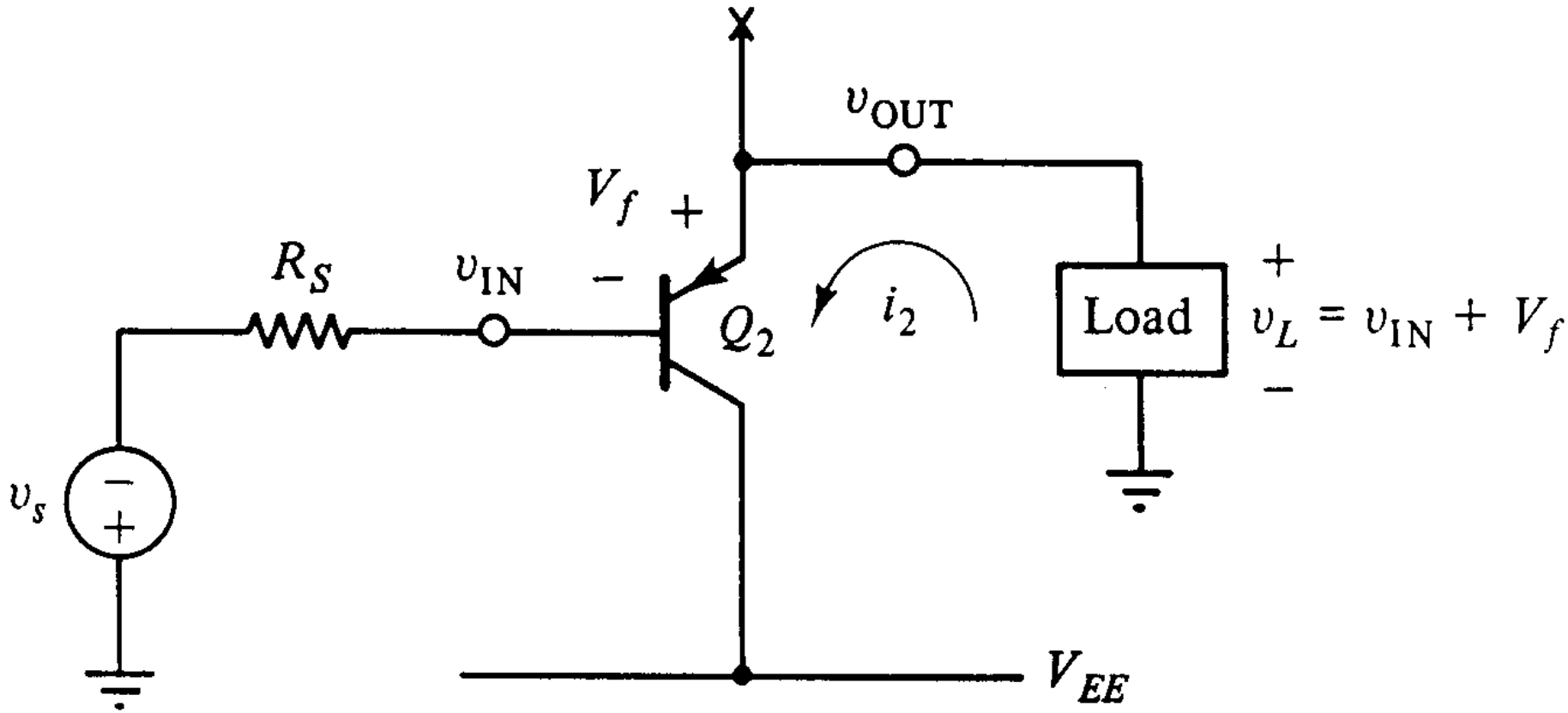


Figure 12.18
Operation of complementary-pair BJT follower for (a) positive ($v_{IN} > V_f$) and (b) negative ($v_{IN} < -V_f$) polarities of v_{IN}. When $|v_{IN}| < V_f$, both Q_1 and Q_2 are in cutoff and $v_L = 0$.

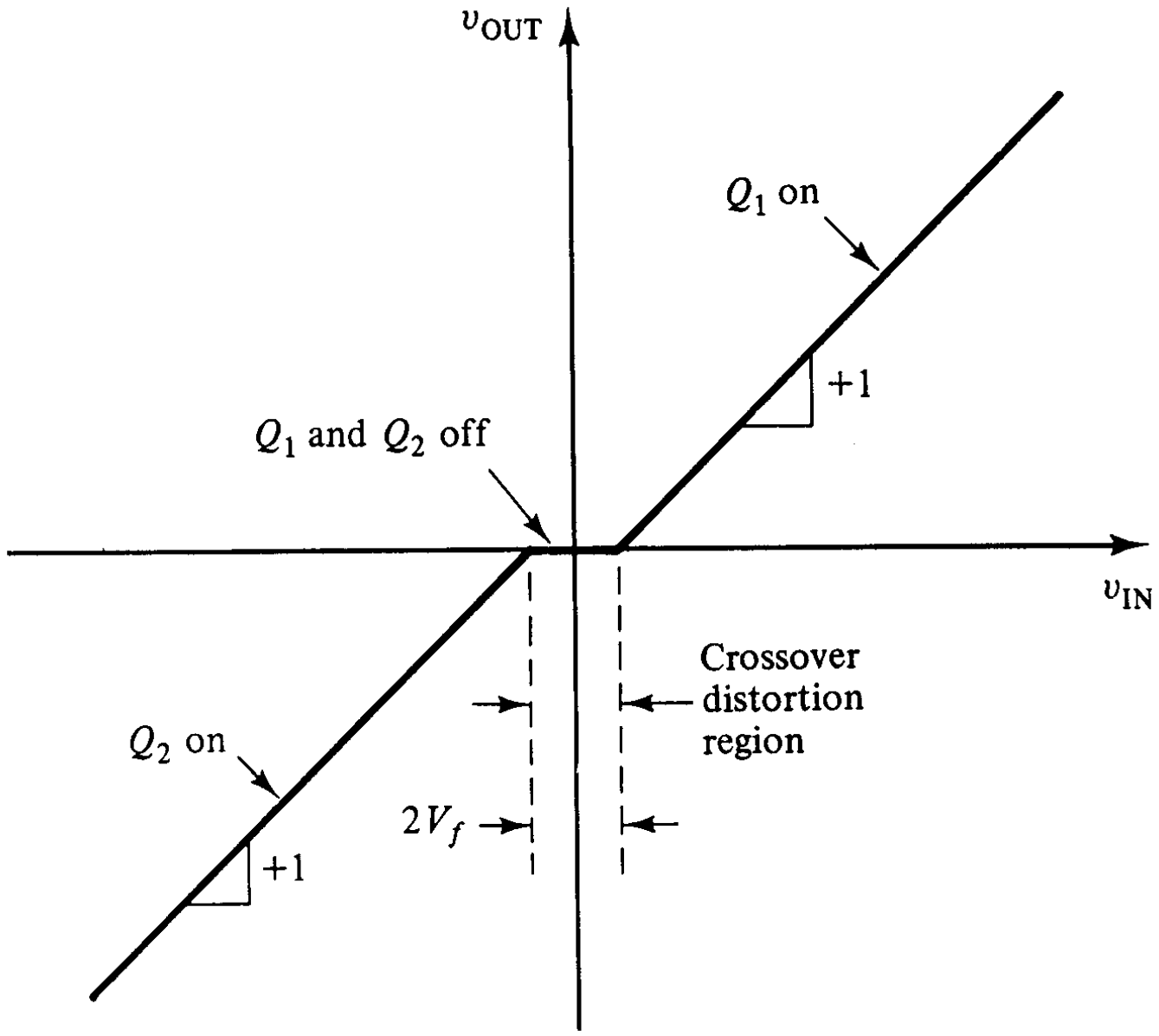


(a)



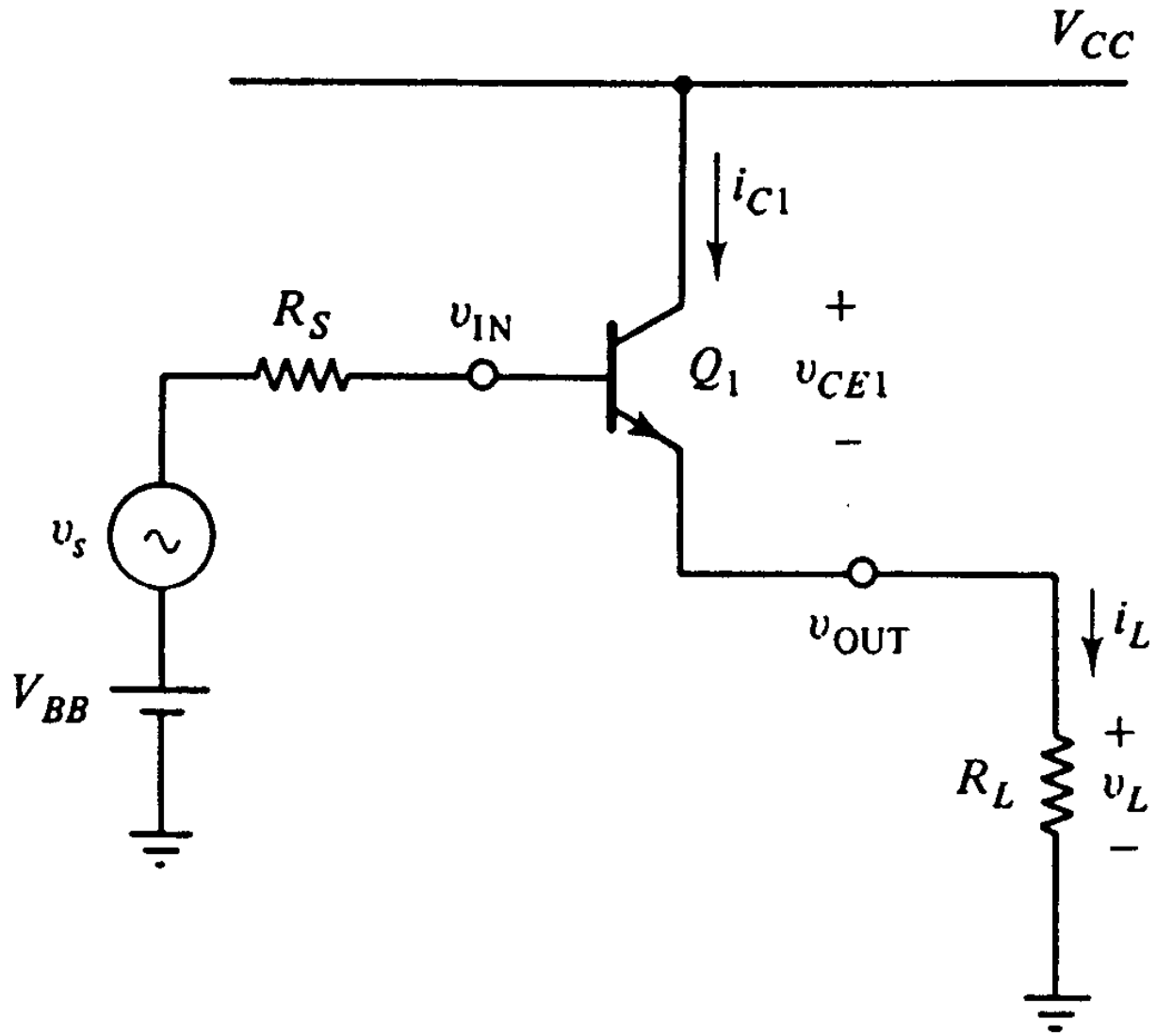
(b)

Figure 12.19
Large-signal transfer characteristic of the BJT circuit of Fig. 12.17. The crossover distortion region has a width of $2V_f$. The slope of the transfer characteristic outside this region is approximately equal to $+1$.



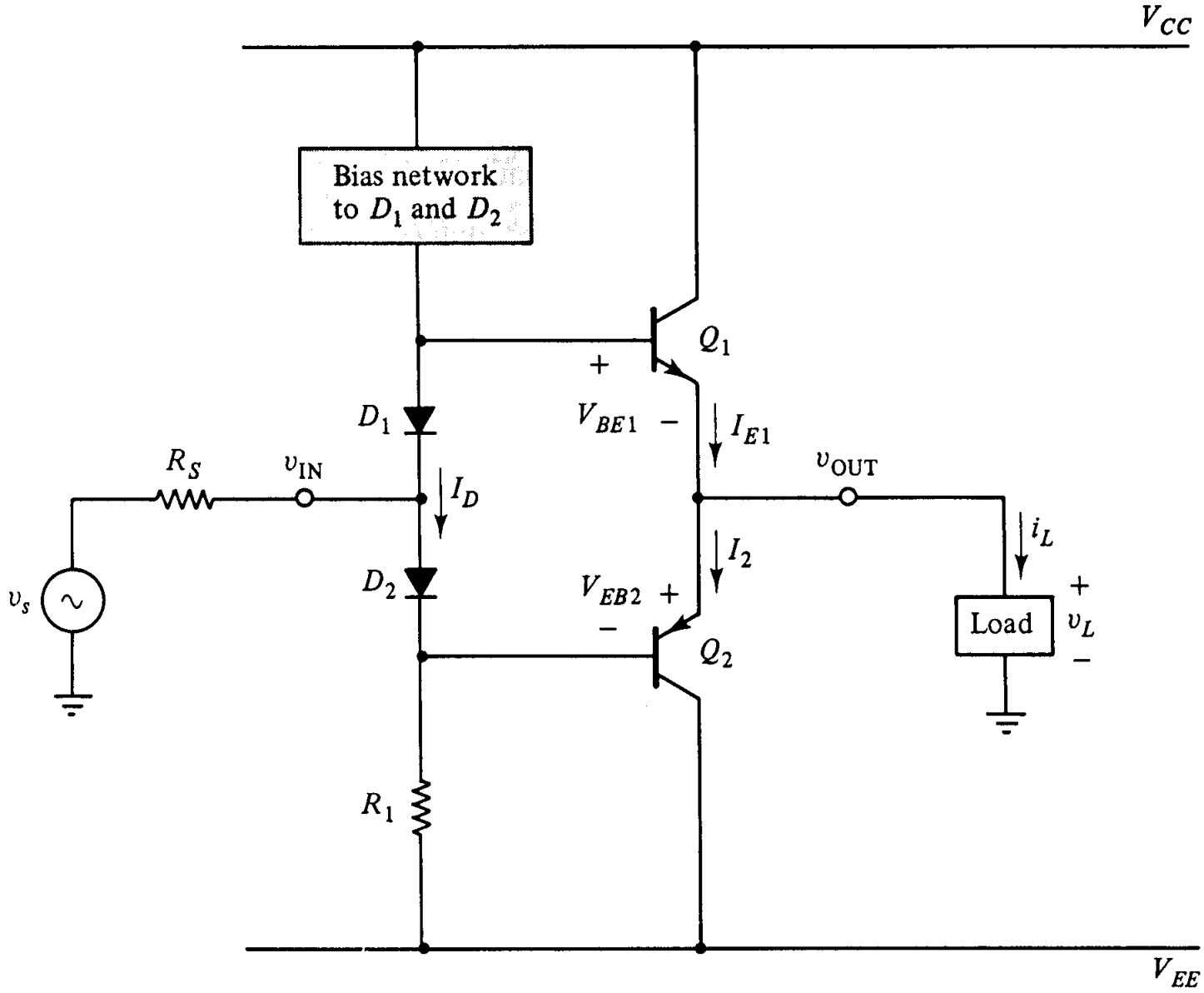
Linearly Biased (Class A) Output

Figure 12.20
One-transistor BJT follower stage. The voltage V_{BB} represents the dc bias voltage fed from the stage preceding the output stage.



Minimally Biased (Class AB) Output

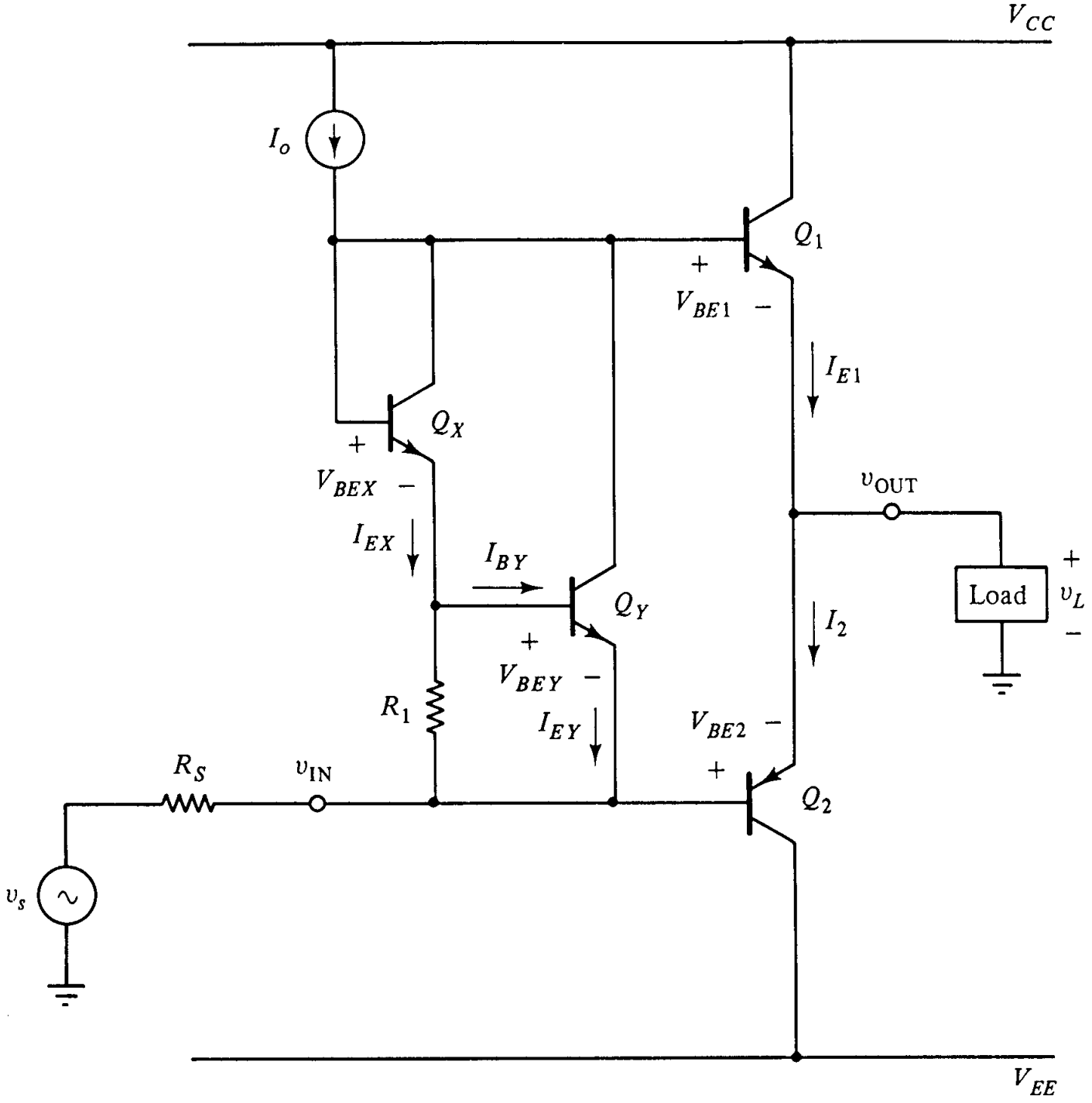
Figure 12.21
Circuit of Fig. 12.17 with diodes added to the base circuit. These diodes bias Q_1 and Q_2 slightly in the active region, forming a class AB amplifier.



Example:

For the following circuit find the bias currents in Q_1 and Q_2 when $I_O = 200\ \mu A$, $I_{EO} = 0.8 \times 10^{-11}$ mA, $R_1 = 40\ k\Omega$.
Assume base currents are negligible.

Figure 12.22
Biasing diodes are replaced by BJTs Q_X and Q_Y.



Assume $V_{BEY}\ 0.6V$ $I_{EX} \cong \frac{V_{BEY}}{R_1} = \frac{0.6V}{40k} = 15\,\mathrm{m}A$

$IEY \cong 185\,\mathrm{m}A$

$$V_{BEY} = \eta\ V_T \ln\frac{I_{EY}}{I_{EO}} = (1)(0.025)\ln\frac{185\,\mathrm{m}A}{0.8x10^{-11}mA}\ 0.597V$$

$$V_{BEX} = \eta\ V_T \ln\frac{I_{EX}}{I_{EO}} = 0.534V$$

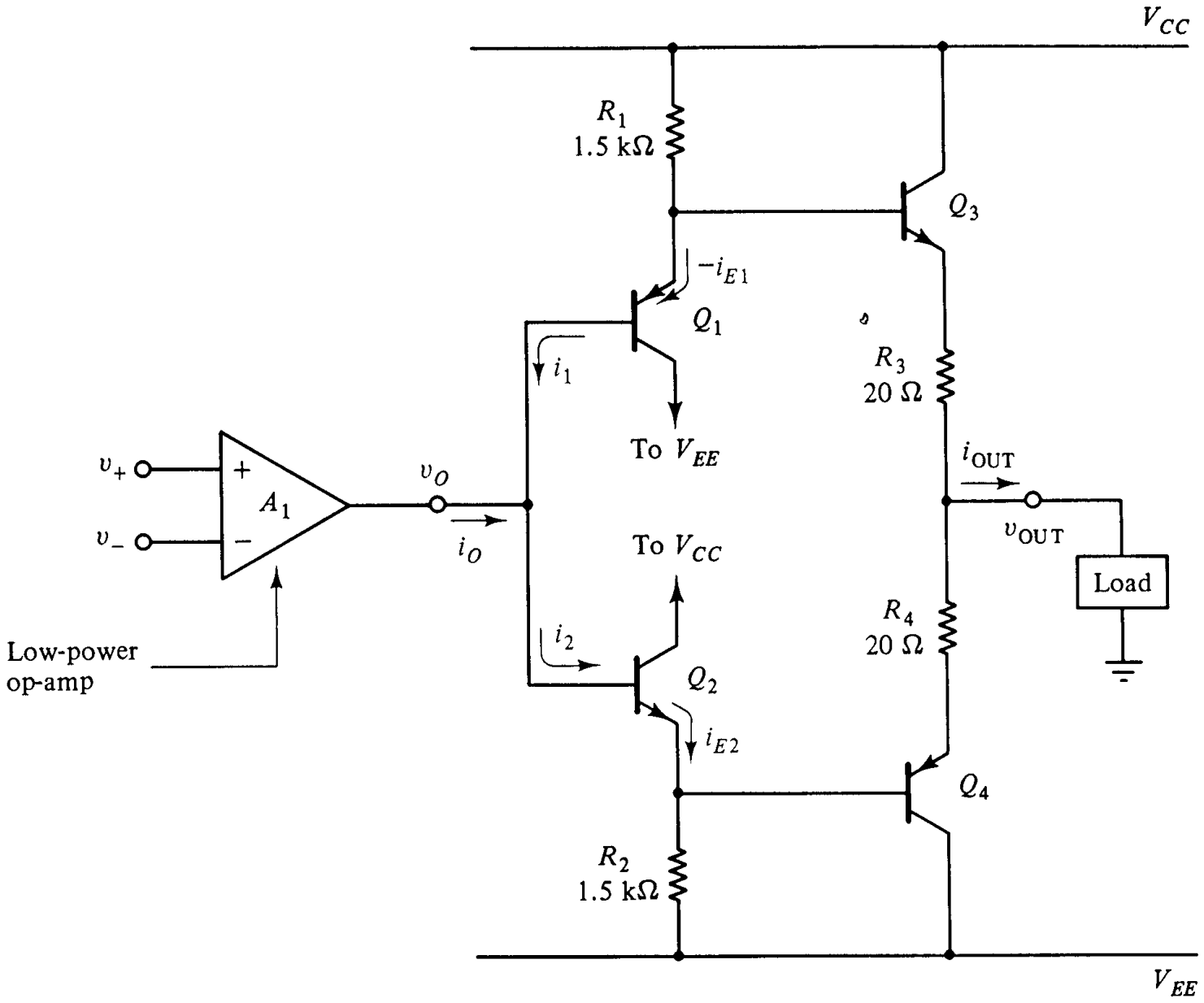
$$V_{BE1} = V_{BE2} = \frac{V_{BEX} + V_{BEY}}{2} = 0.565V$$

$$I_{E1} = I_2 = I_{EO}\left(e^{v_{BE}/\eta V_T} - 1\right) \cong \left(0.8x10^{-11}mA\right)\exp\left(\frac{0.565V}{0.025V}\right) = 53\,\mathrm{m}A$$

Integrated Circuit Power Amplifiers

- A high power device can safely dissipate the heat generated by a large amount of electrical power
- Power amplifiers typically use such high powered devices
- Opamp combined with power amp forms high power opamp which can be connected in usual opamp feedback configurations
- If components are all fabricated on a single chip result is “Integrated circuit power amplifier”
- Advantage of integrated power amp is reduced size and simplicity of use

Figure 12.23
Simplified version of the LH0101 IC power amplifier. All the components shown would be contained on a single IC chip. (Reprinted with permission of National Semiconductor.)



Example:

Consider figure 12.23 with v_{OUT} connected to v_- and v_{IN} connected to v_+ find the output current i_O of the low power opamp A_1 as a function of the output voltage v_O. Assume $V_{EE} = -V_{CC}$.

Solution:

Circuit as connected will function as a voltage follower.

$$v_- = v_{OUT} = v_+ = v_{IN}$$

$$i_O = i_2 - i_1$$

$$i_O \cong \frac{(v_O - V_F) - V_{EE}}{\beta_{F2} R_2} - \frac{V_{CC} - (v_O + V_F)}{\beta_{F1} R_1}$$

$$V_{EE} = -V_{CC},\ R_1 = R_2,\ \beta_{F1} = \beta_{F2}$$

$$i_O = \frac{2v_O}{\beta_{F1} R_1}$$

Example: If $\beta_F = 20, v_{OUT} = 5V, R_{LOAD} = 50\Omega$ Estimate i_{OUT} and i_O

Solution: $$i_{OUT} = \frac{v_{OUT}}{R_{LOAD}} = \frac{5V}{50\Omega} = 100\ mA$$

$v_O \cong v_{OUT}$ Why ?

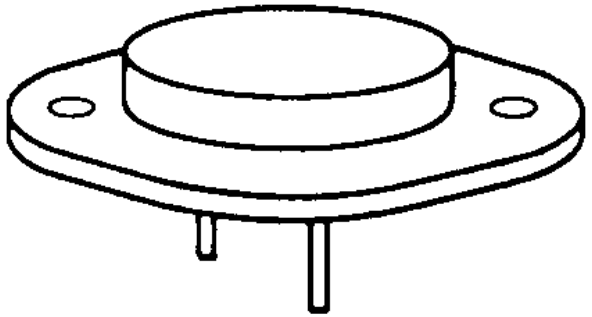
$$i_O = \frac{2v_O}{\beta_F R_1} = \frac{2(5V)}{(20)(1.5k\Omega)} = 0.33mA$$

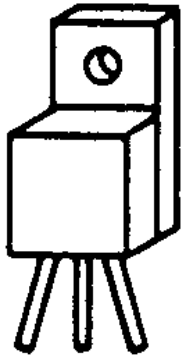
Class AB power amp current gain is $\cong$ 300

Power Devices

- When large amounts of power are delivered to an amplifier load some power will always be dissipated in the transistors of the amplifier
- Power amplifier stage must use specially fabricated power devices capable of safely handling the electrical power dissipated as heat
- Typical device has a large surface area and is mounted in good thermal ambient surroundings

Figure 12.25
Typical high-power device packages.





Heat Sinks

- High power devices are often mounted on metal heat sinks which enhance the overall thermal contact and increase the removal of heat from the devices

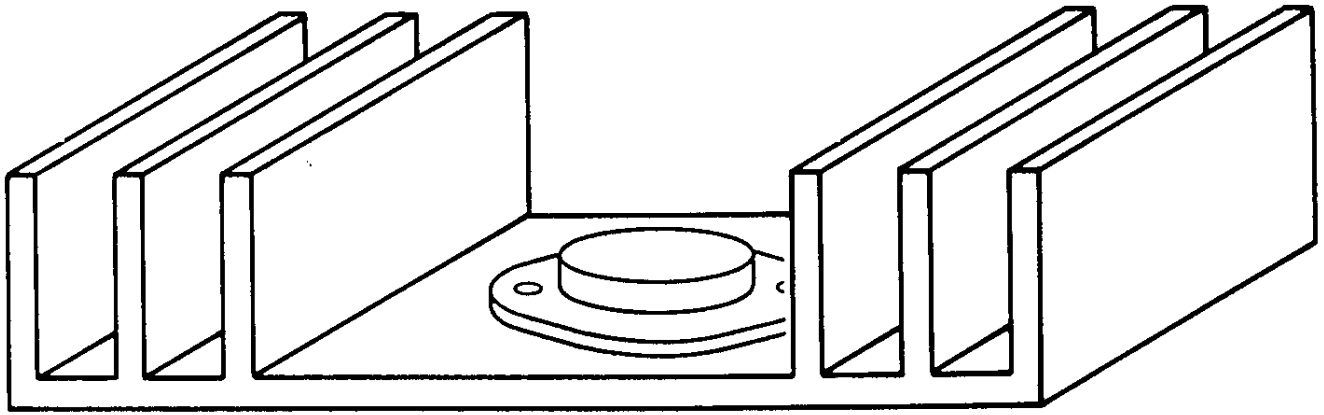


Figure 12.26
Metallic heat sink used to improve the thermal conductivity between a power device and the surrounding air.

- A given heat sink is characterized by the heat transfer coefficient or thermal resistance θ which describes the flow of heat from the sink to ambient air for a given rise in heat sink temperature
- The flow of heat is expressed as energ;y flow per unit time and has units of watts

$$P_{OUT} = \frac{T_{SINK} - T_{AIR}}{\theta}$$

- To improve thermal conduction, heat sinks may be coated with a thermally conductive compound
- If the overall thermal resistance between the transistor case and the heat sink is designed as $\theta_{CASE-SINK}$

$$P_{OUT} = \frac{T_{CASE} - T_{AIR}}{\theta_{CASE-SINK} + \theta_{SINK-AIR}}$$

- The temperature of the semiconductor device will be higher than the case

$$P_{OUT} = \frac{T_{DEVICE} - T_{AIR}}{q_{DEVICE-CASE} + q_{CASE-SINK} + q_{SINK-AIR}}$$

- In thermal equilibrium the electrical power dissipated will equal the heat flow. We can then determine the operating temperature of the device

Example:

A power BJT for which $\theta_{DEVICE - CASE} = 4\ ^{o}\ C / W$ is mounted on a heat sink with $\theta_{SINK - AIR} = 5\ ^{o}\ C / W$. The mounting uses a 0.2 mm thick mica spacer which introduces an additional thermal resistance of $1\ ^{o}\ C / W$ between the transistor case and heat sink. If the BJT carries an average current (i_C) of 1 A at an average voltage of $v_{CE} = 10$ V. Determine the operating temperature of the semiconductor, transistor case and heat sink. Assume $T_{AIR} = 25\ ^{o}\ C$. Neglect power dissipated in the base emitter junction of the BJT.

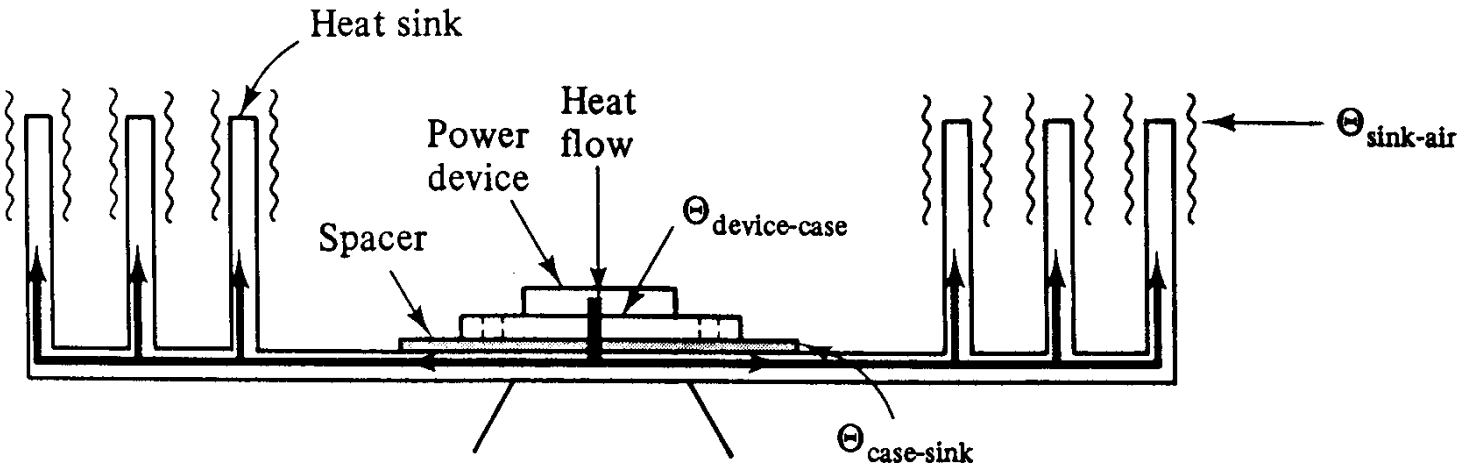


Figure 12.27
Heat flow from power device to ambient air via heat sink.

Solution:

$$P_{ELEC} = i_C\, v_{CE} = (1A)(10\,V) = 10\,W$$

Since $P_{ELEC} = P_{OUT}$ In thermal equilibrium

$$T_{DEVICE} = T_{AIR} + P_{OUT}\left(\theta_{DEVICE-CASE} + \theta_{C-S} + \theta_{S-A}\right)$$

$$= 25\,^{\circ}C + (10\,W)\left(4\,^{\circ}C/W + 1\,^{\circ}C/W + 5\,^{\circ}C/W\right)$$

$$= 125\,^{\circ}C$$

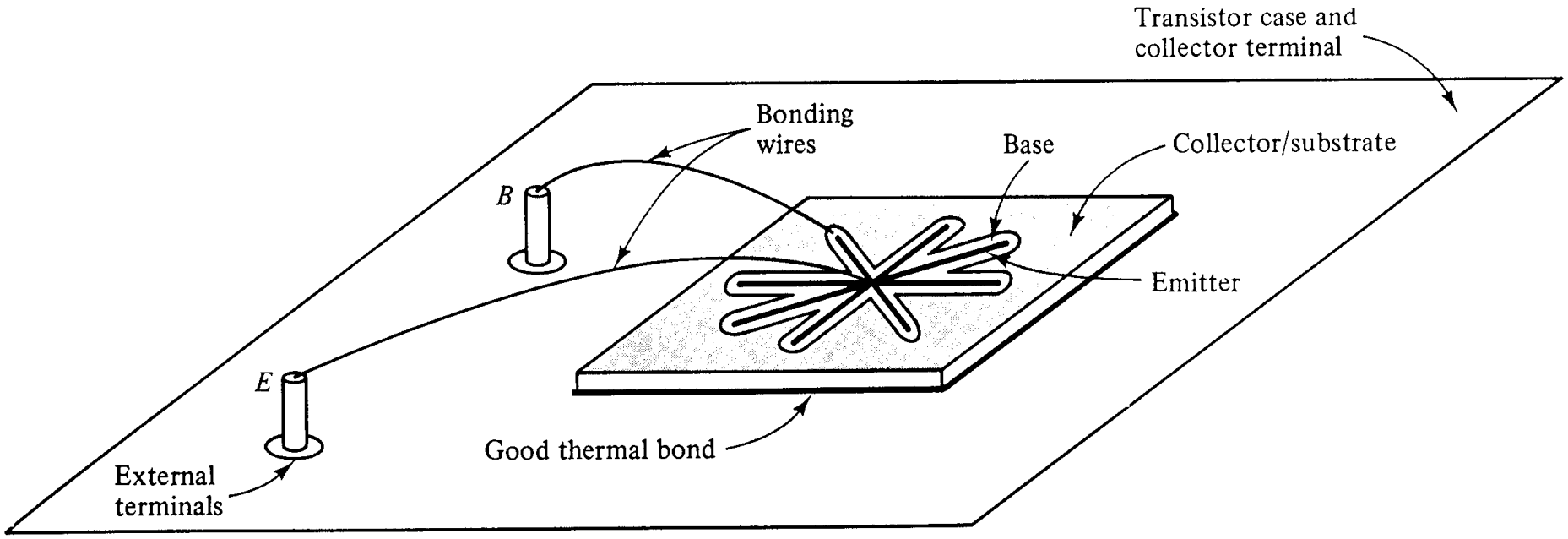
Similarly

$$T_{CASE} = T_{AIR} + P_{OUT}\left(\theta_{C-S} + \theta_{S-A}\right) = 85\,^{\circ}C$$

$$T_{SINK} = T_{AIR} + P_{OUT}\,\theta_{S-A} = 75\,^{\circ}C$$

Power BJT

Figure 12.29 Physical geometry of a typical discrete power BJT.

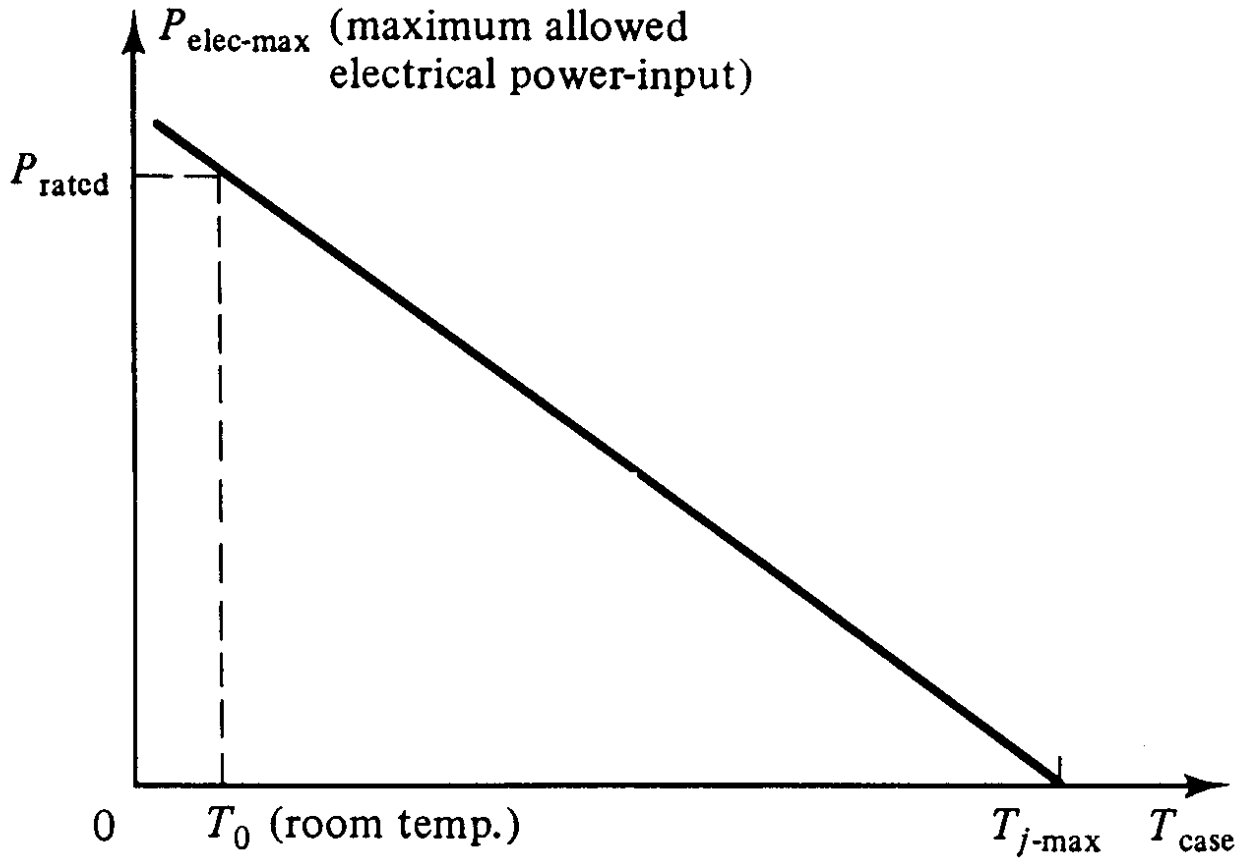


- "Star" shaped pattern of transistor increases surface area of base collector junction where most of the power is dissipated
- Manufacturer usually specifies a maximum temperature $T_{j\text{-}MAX}$ at which the device can be operated without causing permanent damage

$$P_{ELEC-MAX} = \frac{T_{j-MAX} - T_{CASE}}{\theta_{DEVICE-CASE}}$$

- A plot of $P_{ELEC\text{-}MAX}$ versus T_{CASE} is called a power derating curve of the transistor
- The rated power of the device is the maximum electrical power when the case temperature is equal to the room temperature

Figure 12.30
Power transistor derating curve.



- The maximum safe operating power hyperbola is defined for the BJT by the relation

$$P_{ELEC\text{-}MAX} = i_C \, v_{CE}$$

- Note that there are other limiting specs. (e.g. $I_{C\text{-}MAX}$, BV_{CEO}) which may be more stringent than the power operating specs.

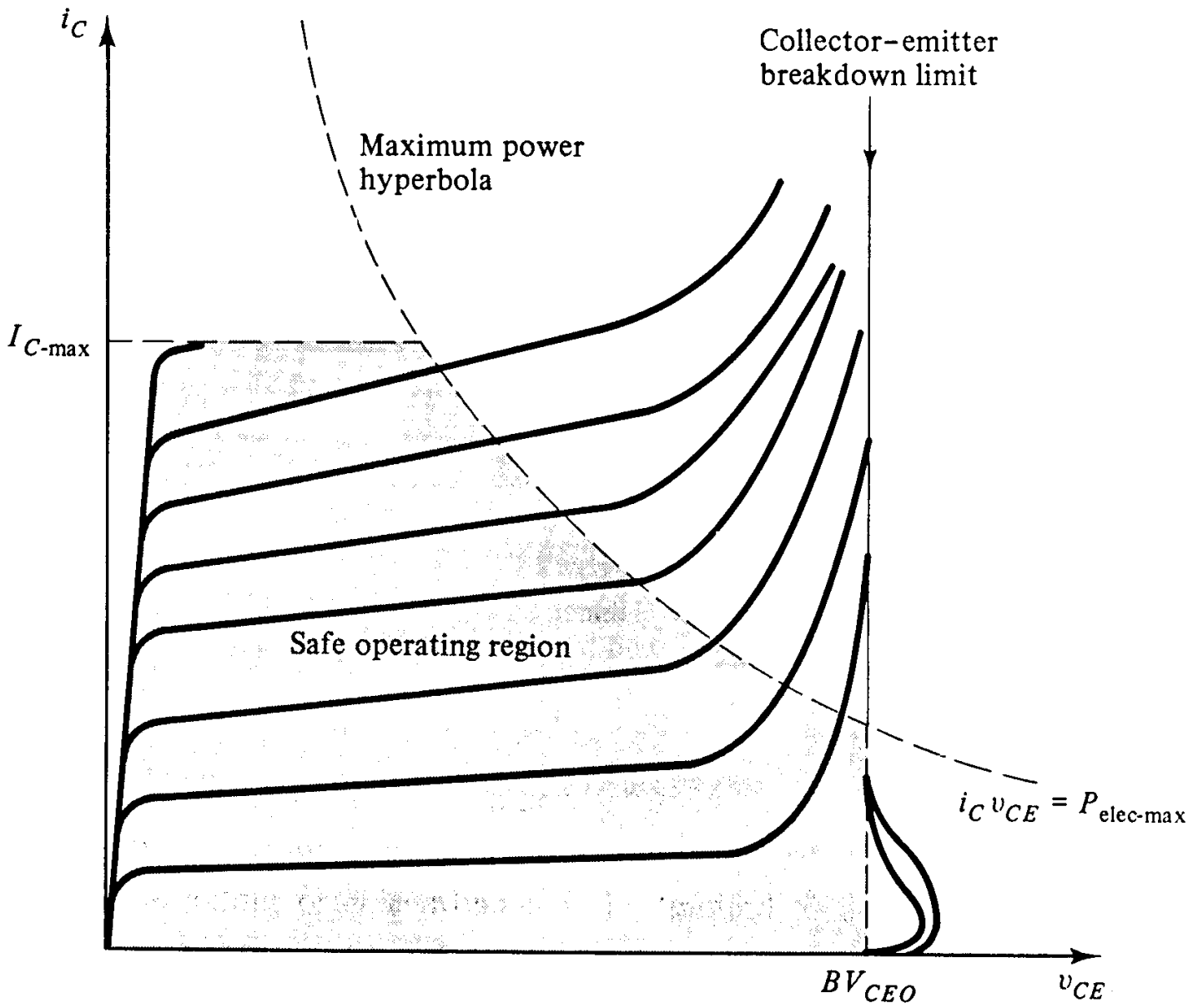


Figure 12.31
Safe operating region of a BJT is defined by the maximum power hyperbola, the maximum collector current $I_{C\text{-max}}$, and the collector–emitter breakdown voltage BV_{CEO}.

Power MOSFETs

- Power MOSFETs are also capable of dissipating large amounts of power
- The planar MOSFET geometry is no longer suitable due to avalanche breakdown in the short channel between drain and source
- Common approach is to use a double diffused vertical MOSFET or DMOS transistor

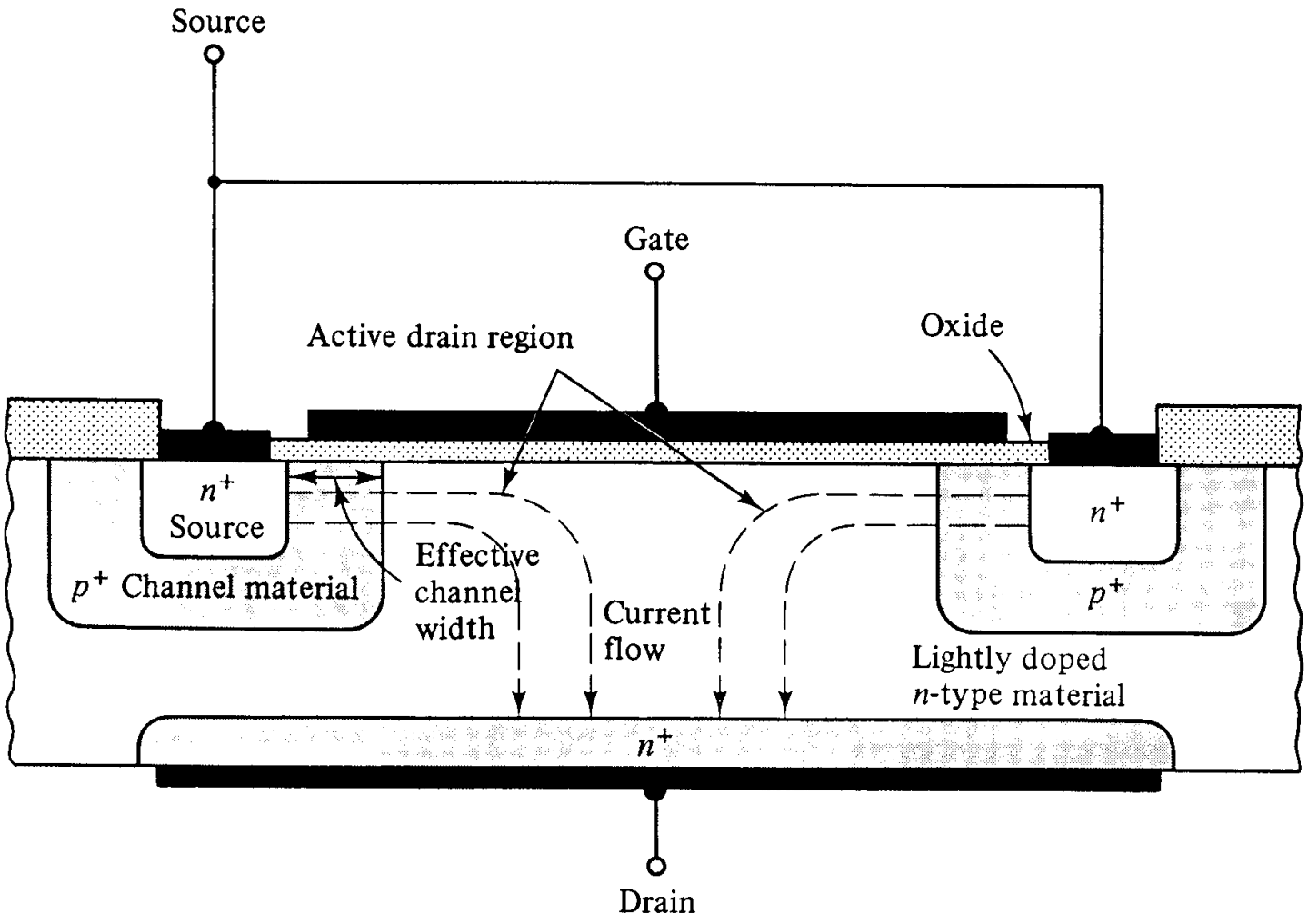


Figure 12.32
Physical geometry of a high-power double-diffused vertical MOSFET (DMOS) device.

Short Circuit Protection and Thermal Shutdown

- The figure below shows a class AB output stage equipped with protection against the effects of short circuiting the output while the stage is sourcing current

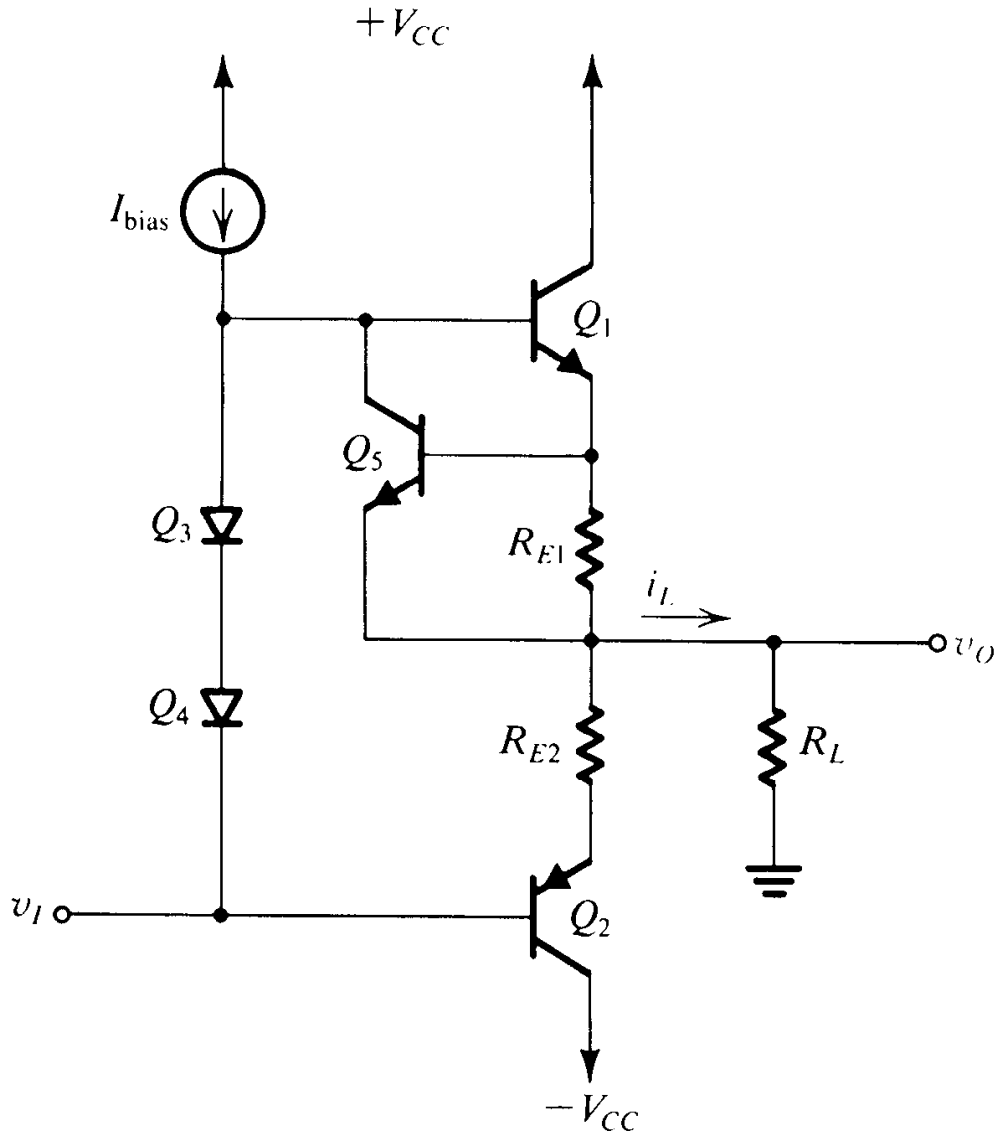


Fig. 9.28 A class AB output stage with short-circuit protection. The protection circuit shown operates in the event of an output short circuit while v_O is positive.

- In addition to short circuit protection most IC power amplifiers are usually equipped with a circuit that shuts the amplifier down if a safe temperature is exceeded

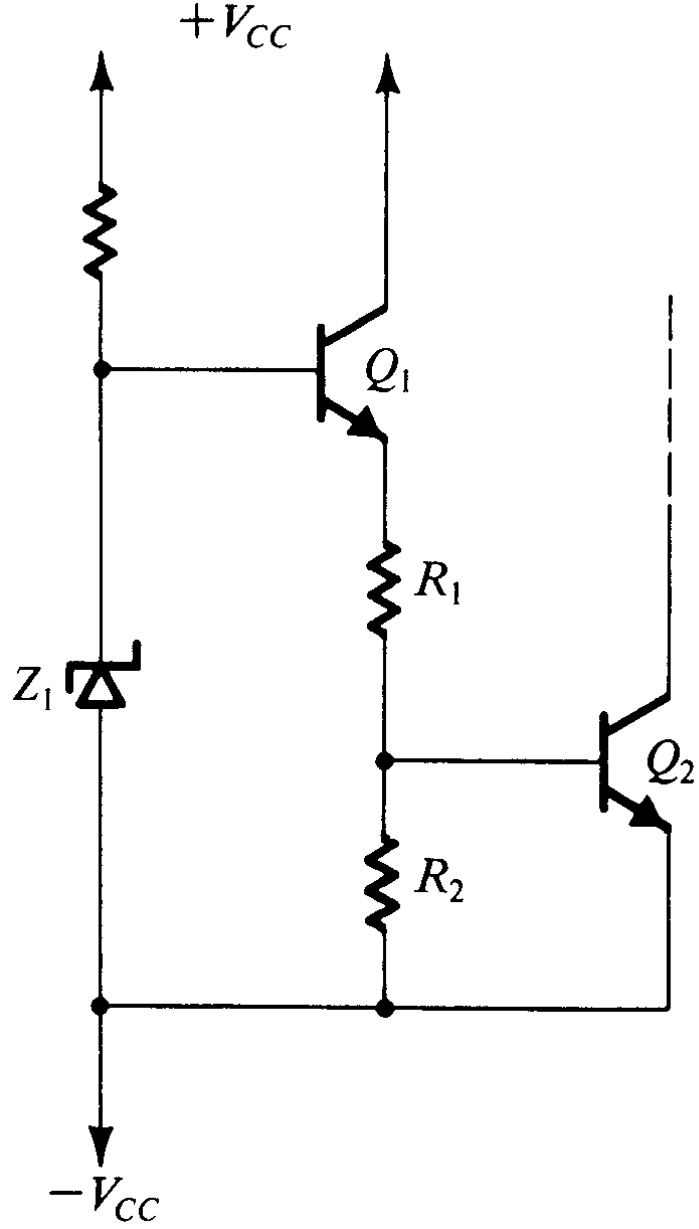


Fig. 9.29 Thermal shutdown circuit.

Feedback and Stability

- An opamp that incorporates negative feedback can be represented by the following block diagram

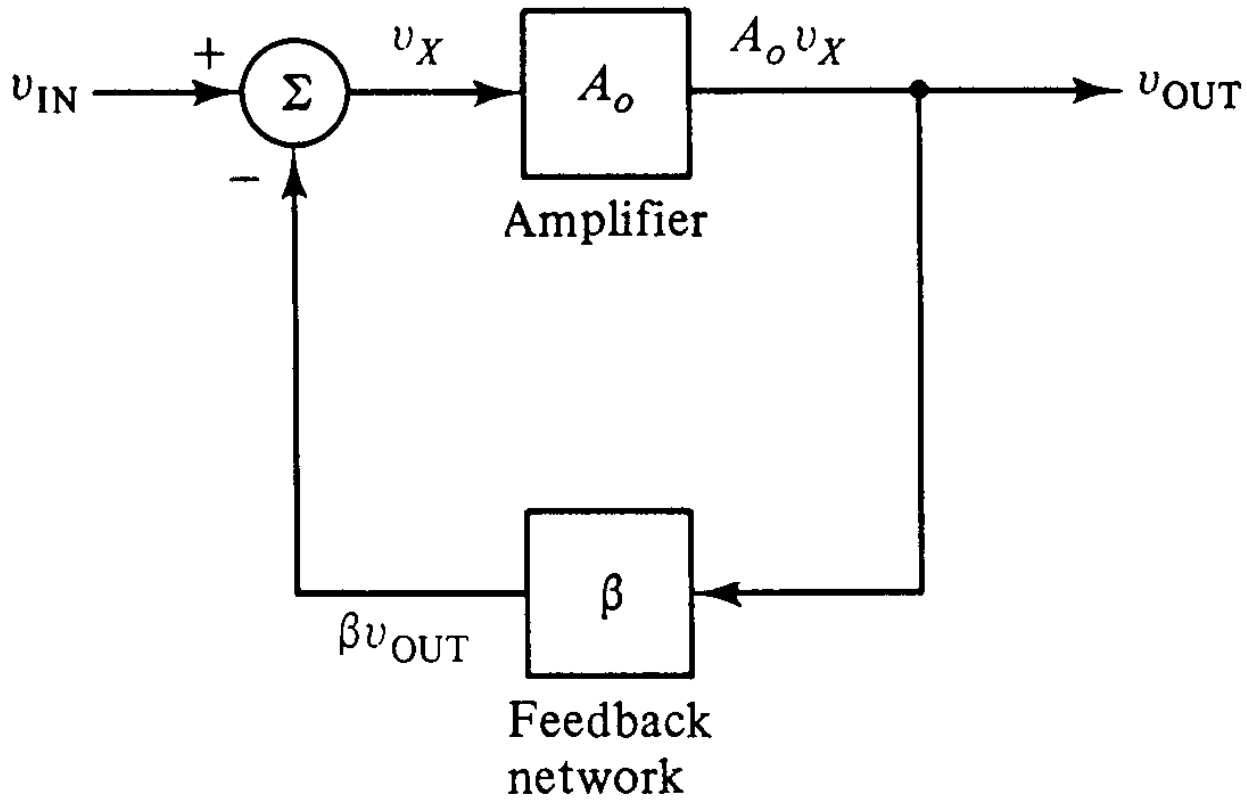


Figure 14.1
Block diagram representation of negative feedback.

- The "amplifier" block multiplies the voltage v_x by A_o which represents the open loop gain of the opamp
- The output of the amplifier is fed into the feedback block where it is multiplied by β. The feedback block represents the components that form the feedback network
- The output of the feedback block is subtracted from v_{IN} and the result is fed back into the amplifier block as v_x

$$v_{OUT} = A_o v_x = A_o (v_{IN} - \beta v_{OUT})$$

$$v_{OUT} = v_{IN}\left[\frac{A_o}{1 + A_o \beta}\right] = v_{IN} \frac{1}{\left(1/A_o + \beta\right)}$$

- The factor multiplying v_{IN} is called the closed loop gain. In the limit $A_o >> 1$

$$v_{OUT} \cong v_{IN} \frac{1}{\beta}$$