ELEC4609 IC PROJECTTESTING- THINGS TO MEASURE March 2017

Before beginning, make some notes on the test set-up. Record equipment models used in testing. Take a photo of the set-up if you wish.

The following assumes you designed the baseline digital pseudorandom bike light controller project.

1. Initially connect a 10 nF capacitor between pads C1 and C2. This relatively small capacitor will give a clock frequency near 1 kHz, making testing simpler.

2. If a reset is necessary, use the Rigol DG-1022 Waveform Generator or the HP4155 to inject a reset pulse with a frequency of 10 Hz or less. Trigger the oscilloscope on the falling edge of the reset pulse. Some projects may not require a reset.

3. Probe the gate of the LED driver output stage. Determine if the expected pseudorandom waveform is observed and select section A or B below accordingly.

A. PRSG Works

1. Record the pseudorandom output waveform. Make sure the complete sequence is shown. You will probably want to record traces on more than one time scale. Look for any "glitches" in the waveform and try to explain them.

2. Using the HP4155 determine the unloaded power supply current IDD drawn from the VDD supply.

3. Probe the phi1 or phi2 line and record the clock rise and fall waveforms on an appropriate time base. Determine the rise and fall times. The oscilloscope probe and cable present a load of about 13 pF.

4. Determine the largest oscillator feedback capacitor for which the full pseudorandom waveform is still obtained. Record the waveform and also note the corresponding oscillator frequency.

5. Connect an LED to the output pad and see if a pseudorandom flash pattern can be seen.

6. Record the voltage waveform at the output pad and estimate the current through the LED.

B. PRSG Doesn't Work

1. Record the waveforms at pads C1 and C2. Compare to Spice simulation.

2. Record the waveform at the phi test pad. Is a suitable clock waveform being generated?

3 Record the waveforms at the phi1 and phi2 test pads. Are these suitable clock waveforms? Are they overlapping?

4 If the phi1 or phi2 waveform is reasonable, record the rise and fall waveforms on an appropriate time base. Determine the rise and fall times. The oscilloscope probe and cable present a load of about 13 pF.

5 Record whatever output waveform your circuit is capable of producing.

6. If your final, submitted layout passed complete LVS and/our extract-and-simulate tests, examine the chip under high magnification with the microscope to attempt to locate photolithography defects (e.g. broken interconnect lines).