An op-amp is a building block required in more complicated analog systems such as switched capacitor filters. The goal of this year's analog project is to integrate a basic op-amp operating from a 3 V supply. A reasonable starting point for the circuit is shown in Fig. 1. This is the basic op-amp discussed in the Baker textbook (p. 618 first edition).

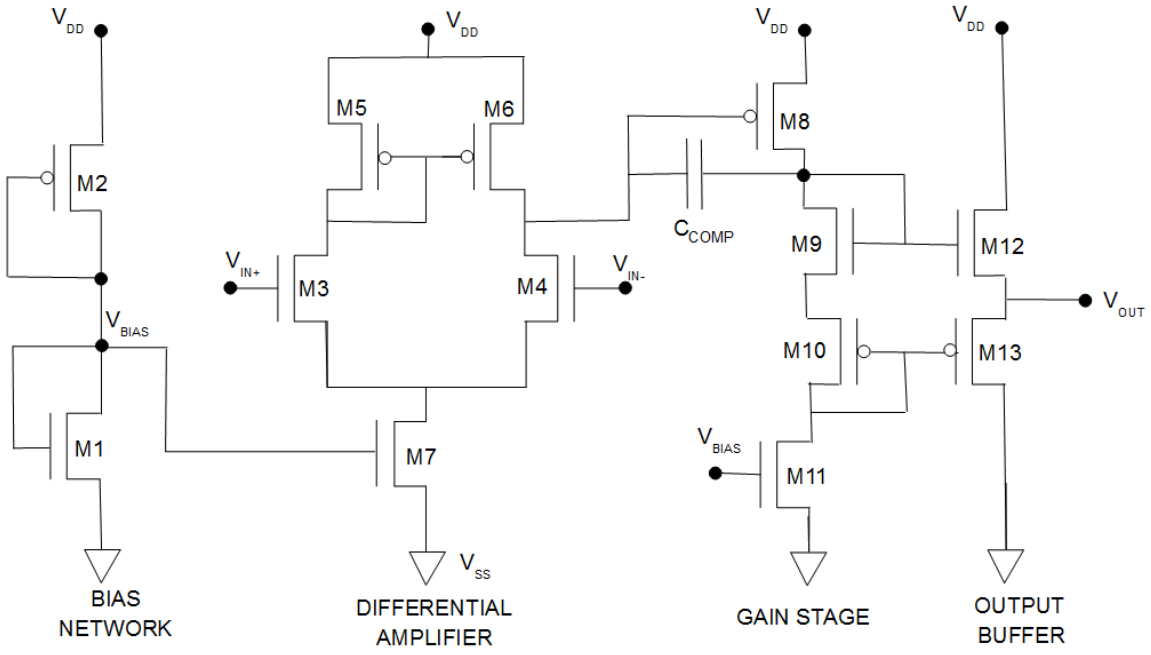

Fig. 1 Basic op amp schematic.

The op-amp has been broken into stages for analysis. Working from left to right, every op-amp will have a bias generation block to provide the DC bias to the current source transistors in the amplifier stages. Every op-amp will also have a differential amplifier stage. The differential amplifier stage here has nMOS driver transistors M3 and M4 with a pMOS current mirror load formed by M5 and M6. Transistor M7 provides a current source for the differential amplifier. Designs with pMOS drivers and nMOS current mirror loads are also common. The differential gain stage is followed by an additional gain stage and then an output buffer intended to provide reasonable current drive into a low-impedance load. The width of the transistors in the output buffer will determine the slew rate of the amplifier, which is an important parameter. There is considerable variation in the design of the gain stage and output buffer. Baker's design uses a pMOS transistor M8 operating as a common source amplifier with nMOS transistor M11 serving as a current source load. Current mirror transistors M9 and M10 connect the output of the gain stage to a push-pull (Class AB amplifier) output buffer formed by M12 and M13. Typically a compensating Miller capacitor (C_{COMP} in Fig. 1) is connected across the gain stage to reduce the gain at high frequencies and provide stability so that the op-amp does not oscillate when used in a closed-loop (feedback) configuration..

At first glance the design of the op-amp may appear to be much simpler than that of the baseline PRSG digital project. There are certainly far fewer transistors to layout. However the choice of *W* and *L* for the transistors requires much more thought and simulation. Minimizing input offset requires precise matching of the transistors in the differential amplifier, something that is not required in a digital circuit. Matching is usually accomplished using common centroid layout techniques (see the “Matching Components” section of the 4609 notes for details). Using a T-gate body contact design (Fig. 2) for the nMOS transistors is desirable to keep I_D constant as V_{DS} increases in saturation.

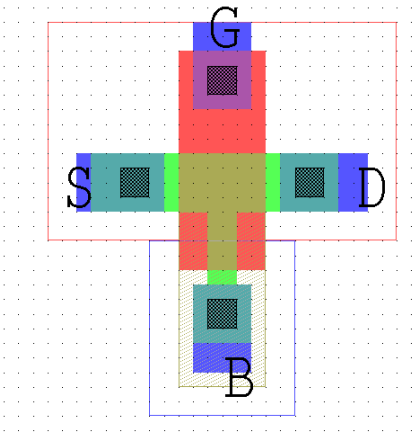

Fig. 2 Example of nMOS T-gate layout

The op-amp is intended to work with the quiescent V_{IN+} and V_{IN-} inputs at analog ground (which we will define as the mid-point between VSS and VDD) and ideally provides an output at analog ground when V_{IN+} and V_{IN-} are both at analog ground.

In a bulk CMOS op-amp the connection of the body terminals on the MOSFETs can have a critical impact on performance. In SOI we can assume the body terminals are connected to the source on each transistor.

Baker suggests beginning the design process by setting a quiescent current of about 20 μA in the differential amplifier and a similar current in the common-source gain stage. This should give an open-loop voltage gain of at least 100. Since the op-amp is normally used in a closed-loop feedback configuration there is no need for higher voltage gain than this. Baker also suggests using widths of hundreds of microns for the transistors in the differential amplifier, but this is excessive for our purposes. A maximum width of about 100 μm is reasonable.

A Bode plot (small-signal gain versus frequency) should be made for the amplifier and C_{COMP} selected to make ensure stability. (The gain should be less than 1 when the phase shift between input and output is about 135 degrees). Achieving stability may be difficult since the maximum size of C_{COMP} is limited to about 10 pF. The only way C_{COMP} can be implemented in the 4609 process is between a poly gate and an underlying channel (nMOS or pMOS). The bias conditions must be such that the channel is always turned on.

Aside from stability, the following parameters should be considered in the design:

a) Maximum output voltage swing (clearly in Fig. 1 the output cannot swing all the way to the V_{DD} or V_{SS} rails since some V_{GS} must be dropped across M12 and M13 to keep these transistors turned on).

b) Common mode rejection ratio CMRR

c) Power dissipation. A quiescent power dissipation around 1 mW is reasonable

d) Unity gain bandwidth

e) Tolerance to process variations. V_{Tn} and V_{Tp} will vary slightly across a wafer and from run to run. Similarly *L* and *W* values will vary since the photolithographic printing process is never perfectly reproducible. A good design will be relatively tolerant of small changes in these parameters.

f) Linearity (1 dB compression)

Project Management

Design of the op-amp will require much more time spent in SPICE circuit simulation than in layout. A suggested approach is to set up schematics for the blocks in Fig. 1 and work out reasonable *L* and *W* values for each block to give acceptable gain. A complete schematic can then be drawn and C_{COMP} selected.

It is recommended that the directive

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.options plotwinsize=0
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be added to the SPICE input file for analog simulations. Usually DC simulations will be used initially to establish bias points, followed by AC simulations to determine gain.

Once the schematic is finalized layout can begin. Component matching should be kept in mind during layout. The layout should also make it possible to probe the outputs of each stage, and override the internal V_{BIAS} generator if necessary. The final layout must fit in the pad frame shown in Fig. 3 below.

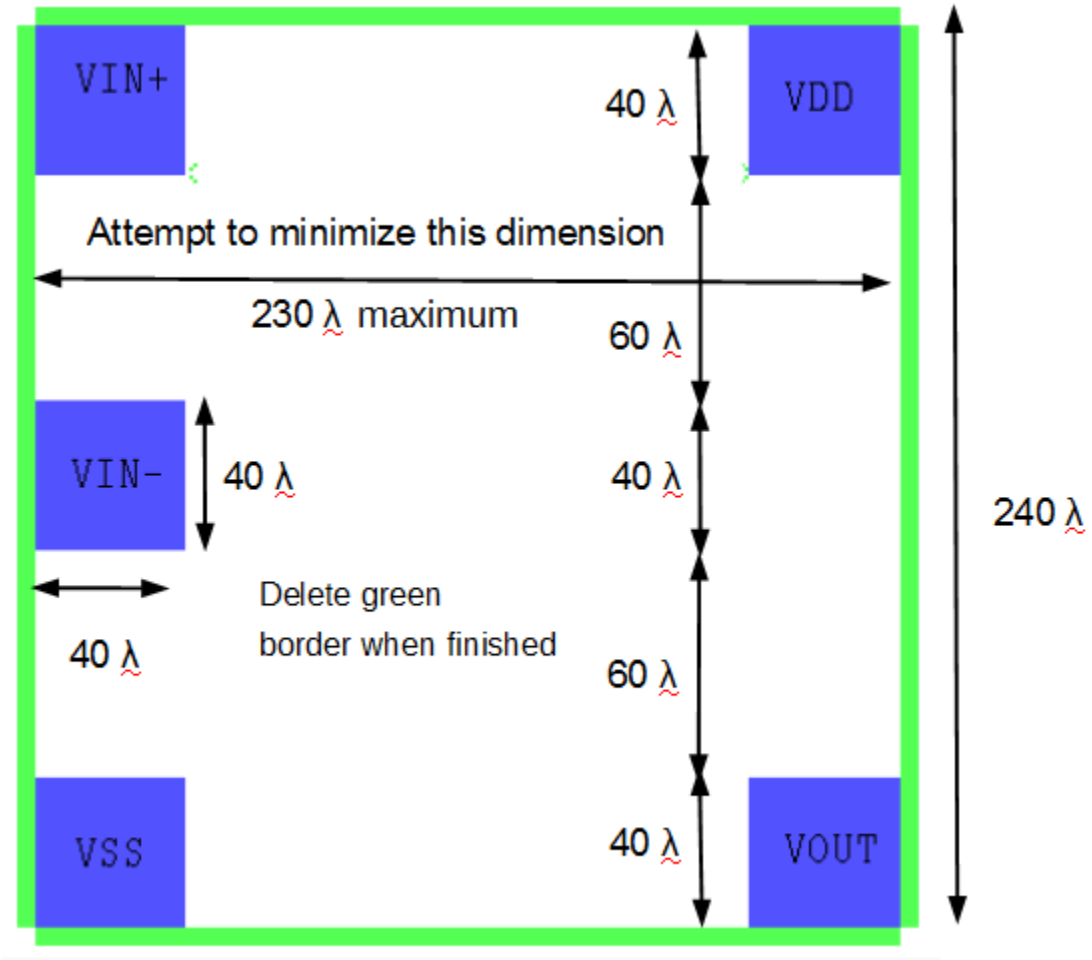

Fig. 3 Pad frame for op-amp project