The 3-bit counter is based on a toggle flip-flop. Here we will use a 2-phase dynamic T-flip-flop as shown in Fig. 1. This is very similar to the D-flip-flop in the baseline project, but an inverted output is provided and the flip-flop output (or the inverted output) is fed back to the input through an nMOS pass gate controlled by the TOGGLE signal. PHI1 and PHI2 are 2-phase non-overlapping clocks. *W*/*L* for the nMOS pass transistors M7, M8, M9 and M10 need to be determined as part of the design process.

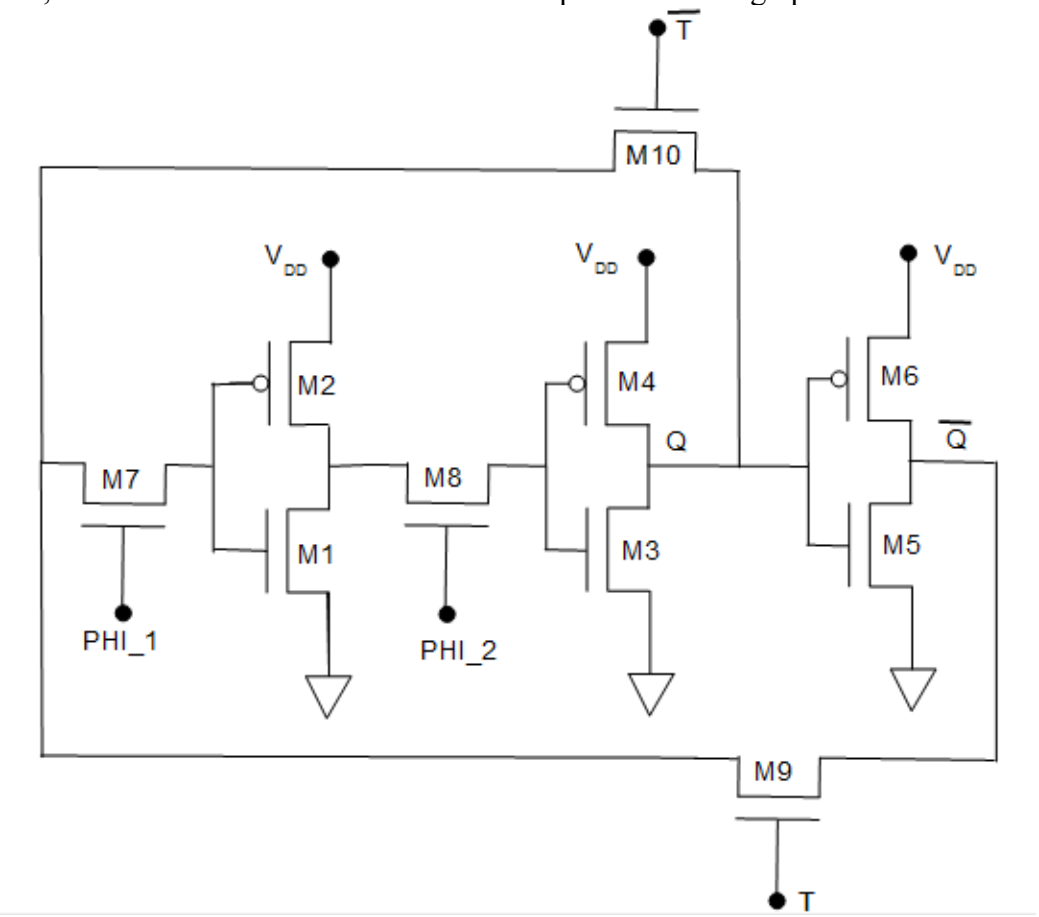

Fig. 1 Dynamic toggle flip-flop

You will need to modify the circuit of Fig. 1 slightly to provide a reset capability for the flip-flop, so that the Q output is forced low when the reset input is high.

To build the counter three T-flip-flops are cascaded, with the toggle signal of each provided by the output of the preceding stage as shown in Fig. 2. The first stage always toggles. Here M101 provides a pull-up to V_{DD}. M102 and M103 pass the toggle command to the next stage. M104 and M105 ensure that the toggle input of each stage is held low unless it is activated by the preceding stage. You will need to determine W/L ratios for all these transistors.

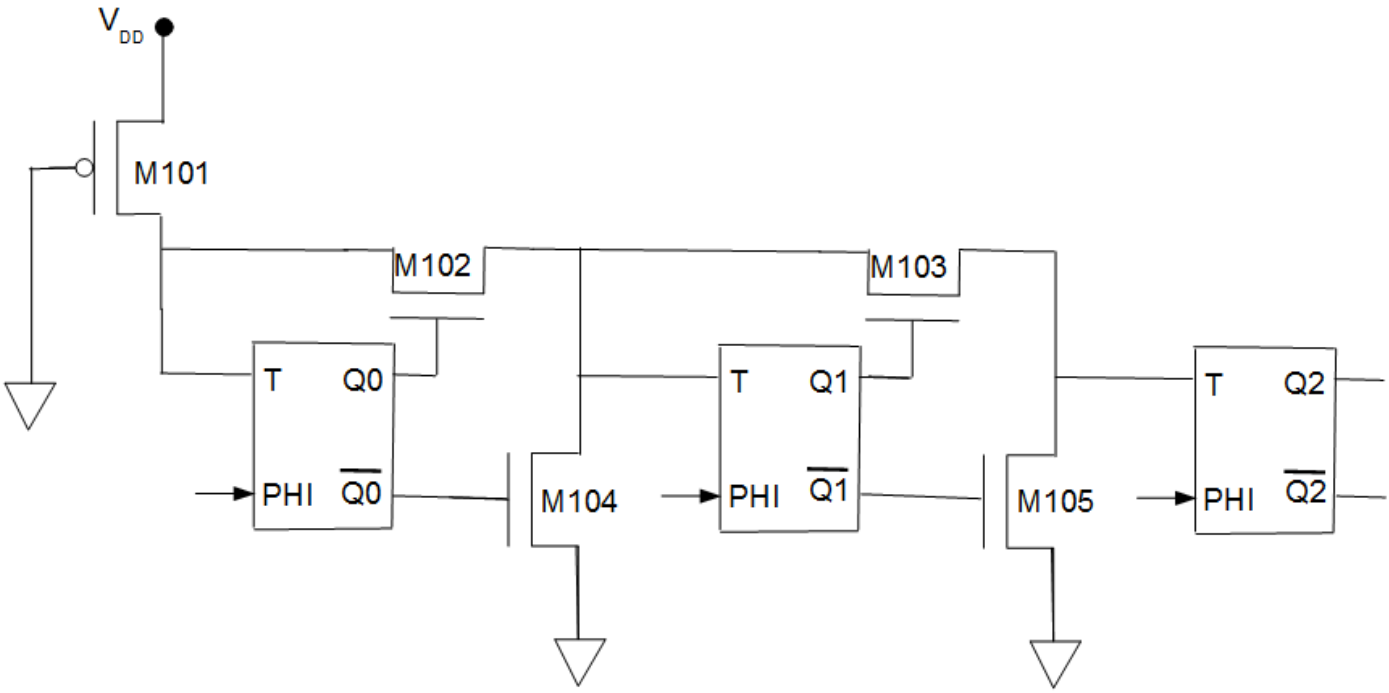

Fig. 2 T-flip-flops cascaded to produce a counter

2-phase non-overlapping clocks φ_1 and φ_2 are required to drive the shift register. These clocks can be generated on chip using the circuit of Fig. 3. The inverters at the output of the NAND gates ensure that φ_1 and φ_2 do not overlap.

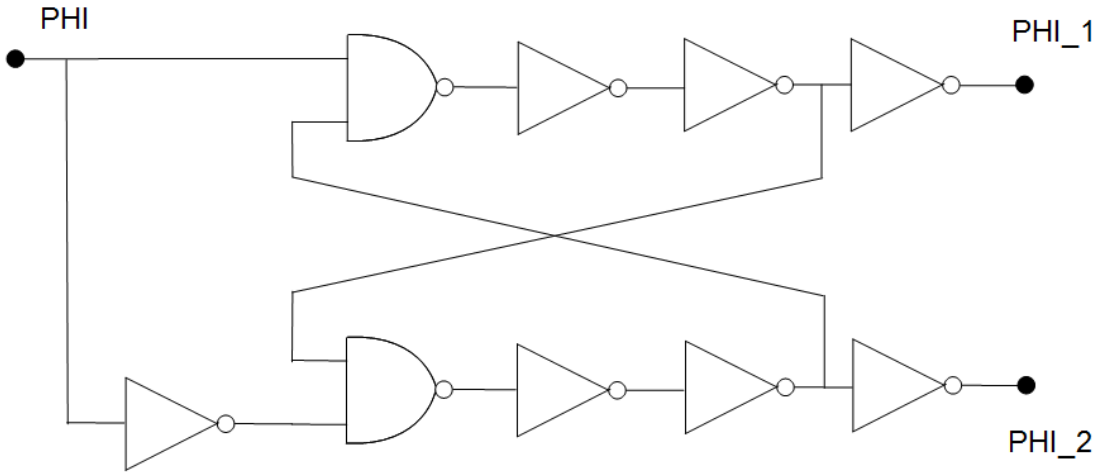

Fig. 3 2-phase clock generator **IMPORTANT NOTE CHANGE!**

The master clock can be supplied from off-chip, or the clock generator circuit shown in Fig. 7 of the baseline project can be used. If the latter approach is taken $C_{external}$ should be chosen to give a frequency of about 1 kHz.

The complete project should include an output buffer optimized to drive a 10 pF oscilloscope probe. Details on how to approach this are given in the notes.

The complete project must fit in the floor plan shown in Fig. 4 which is similar to the cell *frame* in the *cmos2017.tdb* set-up. It will not be possible to probe all the Q outputs simultaneously, but they can be monitored individually with timing compared to timing of the rest pulse. The height of the project block is fixed at 240 λ, and must not be changed. The vertical position of the bond pad centers must also not be changed. The width of the project can be at most 230 λ. There will be rewards for minimizing width.

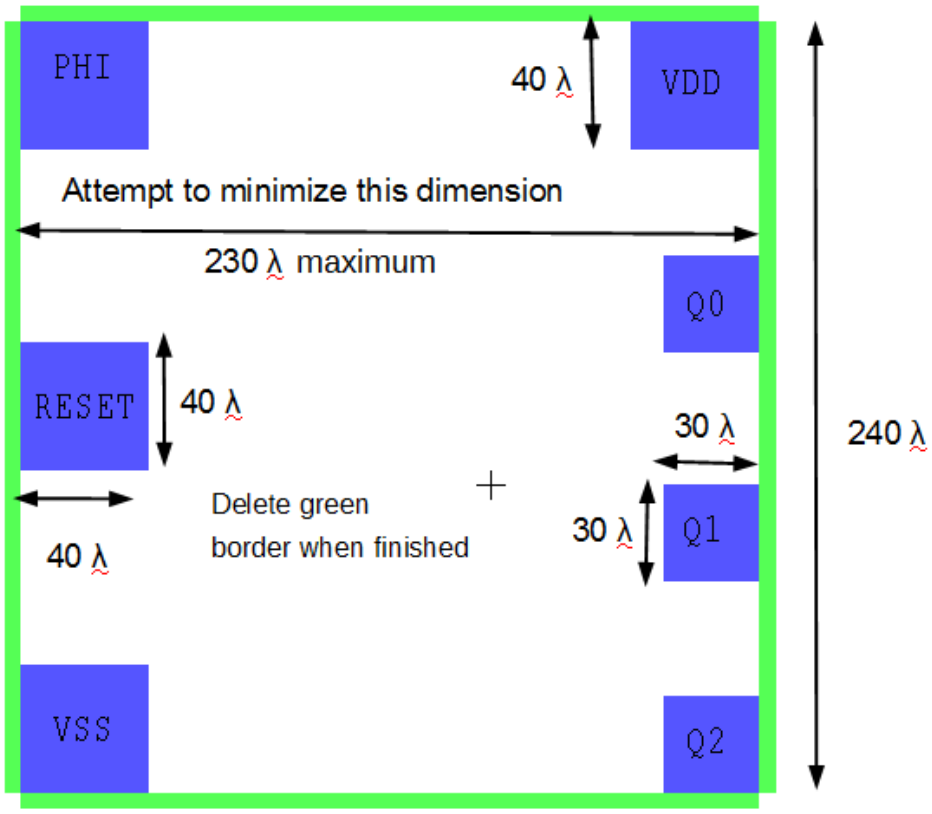

Fig. 4 Probe pad placement and available area for layout

Project Management

It is very important to make an early start on the project. A suggested approach is to draw schematics for each of the following blocks, and then verify the schematics with SPICE simulation:

1. T flip-flop with reset (Fig. 1)
2. 2-phase clock generator (Fig. 3)
3. Output driver

The schematics must include *L* and *W* for each MOSFET. It may make sense to divide up the design of these blocks amongst the partners in a project group..

Once the individual blocks have been verified, a full schematic for the project should be drawn using the blocks as subcircuits. SPICE should be used to demonstrate that the complete circuit is functional (this full schematic and associated SPICE simulation is due on **January 24** and will be worth 10% of the project grade).

To speed up the design process, LTspice schematics for basic NOR and NAND gate subcircuits are available on the 4609 labs webpage.

Once the schematics for each block have been completed, a rough floorplan for the layout should be sketched on paper showing the location of the different subcircuit blocks and routing of the VSS, VDD, clock and reset lines. Each block or cell can then be laid out in LEdit. Once again it probably makes sense to divide up this work between partners. Remember to DRC frequently as you proceed through layout. Once a cell is completed it should be extracted and verified by LVS against the corresponding schematic.

When all the cells have been laid out they can be assembled to produce a final, complete layout. Input protection should be added to the PHI and reset pads (but **NOT** to VSS or VDD) at this stage. The complete layout should then be extracted and verified by LVS and also SPICE simulation of the extracted netlist. The final layout with proof of verification must be submitted by **February 14**.