A Current Folded Down Conversion Mixer in 0.18μ CMOS

Vincent Karam

Project Supervisor Dr. John W. M. Rogers

The submission of this report is for partial fulfillment of the requirement for obtaining

The Bachelor of Engineering degree

Department of Electronics

Carleton University

Ottawa, Canada

April 09, 2003

Acknowledgements

Table of Contents

Lists of Figures

List of Tables

Nomenclature

AC   Alternating Current
C   Capacitor
CMC   Canadian Microelectronic Corporation
DC   Direct Current
dB   Decibels
dBm   Decibels with respect to 1mW
DOCSIS   Data Over Cable Service Interface Specification
DRC   Design Rule Check
DSB NF   Double-Sideband Noise Figure
F   Noise Factor
G_M Transconductance of the Gilbert mixer
g_M Gate Transconductance of a MOSFET
IC   Integrated Circuit
I_D MOSFET Drain Current
IF   Intermediate Frequency
IM3   Third-Order Intermodulation Products
IP3   Third-Order Intercept Point
IIP3   Input-IP3
IR   Image Rejection
IRR   Image Rejection Ratio
L   Inductor
LNA   Low Noise Amplifier
LO   Local Oscillator
LPF   Low Pass Filter
LVS   Layout versus Schematic
MOSFET   Metal-Oxide Semiconductor Field-Effect Transistor
NMOS   N-channel MOSFET
NF   Noise Figure
P1dB   1dB Compression Point
PLL   Phase Locked Loop
RF   Radio Frequency
R   Resistance
RFIC   Radio Frequency Integrated Circuit
PSS   Periodic Steady State
SNR   Signal-to-Noise Ratio
SSB NF   Single-Sideband Noise Figure
SPDR   Spurious-free Dynamic Range
SPSS   Swept Periodic Steady State
TSMC   Taiwan Semiconductor Manufacturing Co.
VCO   Voltage Controlled Oscillator
VOIP   Voice Over Internet Protocol
V_{RF} Voltage Amplitude of RF signal
V_{LO} Voltage Amplitude of LO signal
V_{DS} Voltage of Drain Relative to Source
V_{GS} Voltage of Gate Relative to Source
V_{TH} Voltage of Transistor Threshold

1.0 Introduction

This document entitled "A Current Folded Down-Conversion Mixer in 0.18μ CMOS", is a final report which characterizes the design of a fourth-year project while attending Carleton University. It includes a description of the overall objective of the project, introductory material relating to mixer design and detailed analysis relating to design decisions leading up to the final design.

The objective of this project is to design a completely integrated cable tuner using 0.18μm CMOS technology. The cable tuner is to be used in conjunction with the Data Over Cable Service Interface Specification (DOCSIS) standard which defines interface requirements for cable modems involved in high-speed data distribution over cable television system networks. In the near future, cable tuners will support continuous broadband internet connectivity, telephony, video conferencing and voice over IP (VOIP).

The fourth year project will be supervised by Dr. John Rogers; my task will be to design a down-converting mixer stage of the cable tuner. The tasks of the design team are tabulated below.

Table 1: Cable Tuner Project Participants

Member	Contact	Delegation
Vincent Karam	karam@magma.ca	IR Mixer (Gilbert Cell)
Derek van Gaal	dvgaal@chat.carleton.ca	IR Mixer (LNA, 90˚ Shifter)
Mark Fairbairn	mfairbai@chat.carleton.ca	Frequency Synthesizer
Christina George	chrissyge@yahoo.com	Low Noise Amplifier
Kevin Cheung	kcheung@chat.carleton.ca	Voltage Controlled Oscillator
Bi Pham	bpham@chat.carleton.ca	Primary Mixer

2.0 Background

The design of the cable tuner will consist of three major sections, a wide-band radio frequency (RF) font-end tuner (47-870MHz), an image-reject (IR) mixer intermediate frequency (IF) stage and synthesizer design (includes, voltage controlled oscillator (VCO) and phase locked-loop (PLL) design).

The front-end of the tuner consists of a low noise amplifier (LNA), a low pass filter (LPF) and a high linearity mixer. In order to meet system requirements, this section must be able to support high bandwidth and maintain low power consumption. It is also necessary that this block will assume high linearity and low noise. The overall design of the cable tuner will be comprised of a fully differential design in order to alleviate the noise constraints. In the case of the second section, the IR mixer, noise contributions, amplitude and phase mismatch and gain will be the significant limiting factors to the overall design. The synthesizer stage will include dual Phase Lock Loops (PLL) in order to accommodate the channel selection mixer and the IF down-converting mixer. The tuner should be able to support 256-QAM digital formats in order to enhance the use of bandwidth.
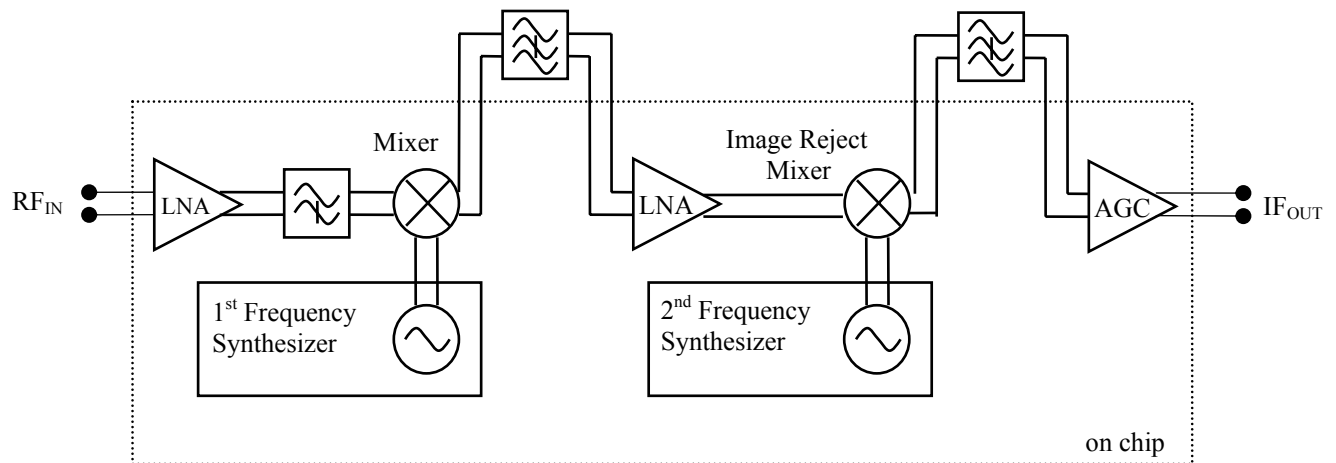

Figure 1: Integrated Cable Tuner Architecture[1]

3.0 Mixer Theory

3.1 Introduction

Mixers are essential to most communications systems as they perform the necessary frequency translation of signals. Most information signals travel at frequencies much larger than that of human speech or digital data in order to maximize bandwidth and minimize propagation power and antenna size. Frequency translation is also done to make effective use of bandwidth and organization of frequency allocations for different types of propagating signals. This high frequency or radio frequency (RF) must be down-converted back into a lower intermediate frequency (IF) so that the data can then be interpreted. This down-conversion is realized by the multiplication of the incoming RF signal by a local oscillating (LO) frequency. [2]

Mixers are unique in the sense that they are one of the few components in a communication structure that are required to be non-linear. Non-linear mixer behaviour can be achieved in several ways; most common non-linear circuits take the form of diodes, switching modulators such as choppers or analog multipliers such as a Gilbert cell. The basic functionality of the mixer operation relies on the multiplication of two signals in the time domain.
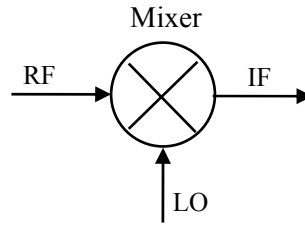

Figure 2: Down Converting Mixer Model

$$V_{RF} = A\cos(\omega_{RF})t$$
$$V_{LO} = B\cos(\omega_{LO})t$$

$$V_{IF} = A\cos(\omega_{RF})t)*(B\cos(\omega_{LO})t$$
$$V_{IF} = \frac{AB}{2}[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} - \omega_{LO})t]$$

where,
  A and B are constants

3.2 Linearity

The non-linear properties of circuitry can be described in the following power series equation:

$$v_o = k_0 + k_1 v_{in} + k_2 v_{in}^2 + k_3 v_{in}^3 + k_4 v_{in}^4 ...$$

where,

$$v_{in} = x_1 + x_2 = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$$

Noting that the first three terms will yield a sufficiently accurate characterization, the output of the power series equates to:

$$v_o = k_0 + k_1(x_1 + x_2) + k_2(x_1 + x_2)^2 + k_3(x_1 + x_2)^3$$

$$v_o = k_0 + \underbrace{k_1(x_1 + x_2)}_{\text{fundamental}} + \underbrace{k_2(x_1^2 + 2x_1 x_2 + x_2^2)}_{\text{second order}} + \underbrace{k_3(x_1^3 + 3x_1^2 x_2 + 3x_1 x_2^2 + x_2^3)}_{\text{third order}}$$

The expanded second order and third order terms are:

$$(x_1 + x_2)^2 = (x_1^2 + 2x_1 x_2 + x_2^2)$$
$$\text{HD2}\quad\text{MIX}\quad\text{HD2}$$

$$(x_1 + x_2)^3 = (x_1^3 + 3x_1^2 x_2 + 3x_1 x_2^2 + x_2^3)$$
$$\text{HD3}\quad\text{IM3}\quad\text{IM3}\quad\text{HD3}$$

The second order term MIX, also known as IM2 (second order intermodulation) produce the nonlinearity needed for frequency translation. The undesired terms HD3 and IM3 produce undesired nonlinear effects such as gain compression and intermodulation distortion. These effects will be discussed in the following sections.

3.3 Third Order Intercept Point IP3

Although mixers are based on a fundamental non-linear principle, it is important that the mixer must also be able to amplify a range of incoming signals in a linear fashion. A commonly used measure of linearity is the third order intercept (IP3) point. This measure describes the real-world scenario of having two input signals spaced relatively close together on the frequency spectrum fed into the mixer, one being the desired signal in the channel of interest and the other being the undesired signal (an interfering signal of the adjacent channel). The collaborated effects of these signals are known as intermodulation. Most critical are third-order intermodulation (IM3) components that appear at the output of the mixer, their frequencies of $2\omega_{RF1}$ - ω_{RF2} and $2\omega_{RF2}$ - ω_{RF1} may lie within the passband of the desired IF, subsequent to mixing operation. The undesired intermodulated signals are amplified by a non-linear cubic relationship to the input signal strength. Ideally this is to say that as the RF input power increases, the output power of the undesired IM3 signals will intersect the output power of the desired signal. It is this intersection that is referred to as the IP3 point. In reality, since either of the signals will saturate and this intercept point will never occur, however an extrapolation of their linear slopes will serve as a good estimate. If the IP3 is referenced to the input power of the mixer, it is known as the input third-order intercept point (IIP3). [3]

3.4 1dB Compression Point

Characterization of linear behaviour in RF circuits requires quantification of the maximum input range for a given design stage. Ideally one would like the output power to be linearly proportional to a given input power. However, due to the effects of noise and intermodulation distortion, mixer behaviour will deviate from desired linearity, entering a region of saturation or compression. The 1dB compression point is simply described as the point where the output power is 1dB less than that of the ideal gain for a given input power. [3]

3.5 Spurious Free Dynamic Range (SFDR)

Since mixers can accommodate a wide range of signal strengths, (weak signals are governed by the noise floor while strong signals are governed by the 1dB compression point) a measure is introduced so as to quantify the overall usable range, known as the spurious-free dynamic range (SFDR). The SFDR of a system is defined as a ratio where the input power level is distinguished by the intersection of the IM3 term and the minimally detected signal. [4]
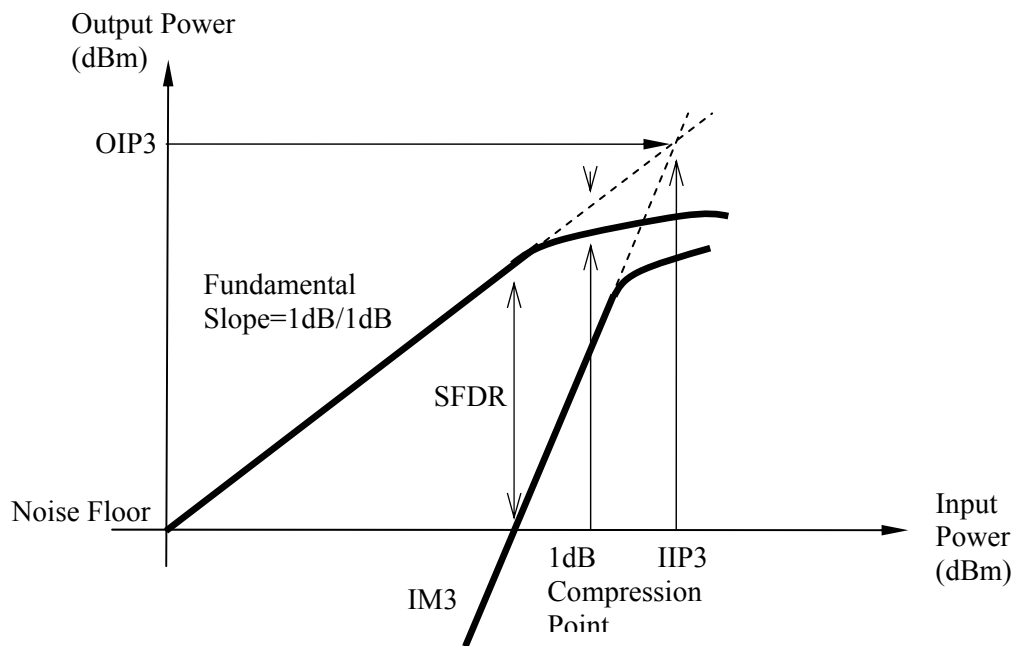

Figure 2: Distortion vs. Power Level

3.7 Noise

In any electrical circuit, signals are subject to degradation and corruption due to the negative effects of physical interaction between traveling electrons. A measure of input noise corruption relative to output noise corruption is called the noise factor (F), if measured in decibels it is known as the noise figure (NF). [5]

$$F = \frac{(S/N)_{IN}}{(S/N)_{OUT}} = \frac{GN_{IN} + N_{added}}{GN_{IN}}$$

where:

(S/N) is the signal to noise ratio

N_{added} is the noise added by circuitry

$$NF = 10\log(F)$$

In the context of mixers there are two main frequencies that contribute to the IF output signal, the desired RF signal and the undesired image signal (IM). If one is only interested in the information carried by the desired RF signal then the noise figure is referred to as the single-sideband noise figure (SSB NF). Since the SSB has signal power in only one sideband and both measures contribute the same amount of IF noise, the SSB NF will amount to 50% or 3dB higher than that of the DSB NF. [3]

3.8 Double Balanced Gilbert Mixer

The basis of mixing relies on the multiplication of two signals, we will assume an ideal square wave, the LO signal and an incoming information signal, the RF signal. The voltage of the RF signal is amplified and converted into a current by a driver stage. The LO signal is used to steer all of the current from one transistor to the other at the LO switching stage. Finally, the IF output voltage is created due to the current through the load resistors. Refer to Figure 3 for an illustrated diagram of a double balanced mixer.

The most common of mixer topologies is the double balanced configuration known as the Gilbert Cell. This design is often chosen over the simpler single balanced configuration due to it's LO feedthrough isolation properties. Double balanced mixers use symmetry to cancel unwanted LO components while enhancing desired mixing components at the output.
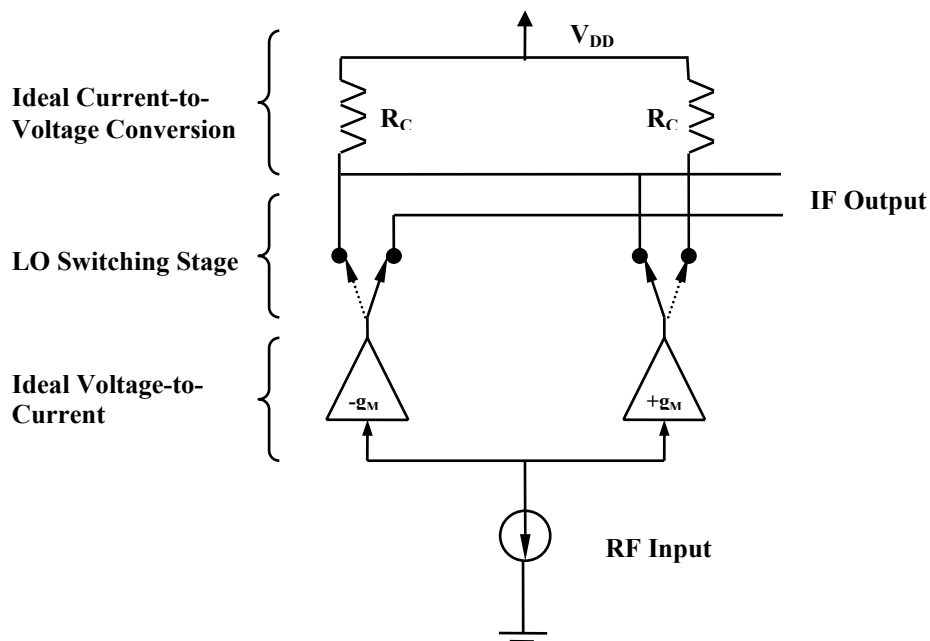

Figure 3: Ideal Double Balanced Mixer

4.0 Image Reject Mixer Design

4.1 Introduction

The purpose of the image reject mixer is to down-convert a pre-selected channel frequency from 1.9GHz to 50MHz. It is essential to the overall operation of the mixer that linearity and gain of the incoming RF signal is maximized at the output, and that noise and power consumption are minimized. These four parameters will be optimized throughout the design process such that the performance characteristics of the final design fall within the specification limits. Figure 4 illustrates the system level design of the image reject mixer. Note that the mixer is of a differential nature and exploits the Hartley architecture. The phase of the RF input signal is mixed with the quadrature of the LO signal. That is to say that the operation of one mixer is always 90º from the phase of the other. Their phases are then realigned and summed at the output; this technique serves to eliminate even-order distortion and provide effective image cancellation. [4]
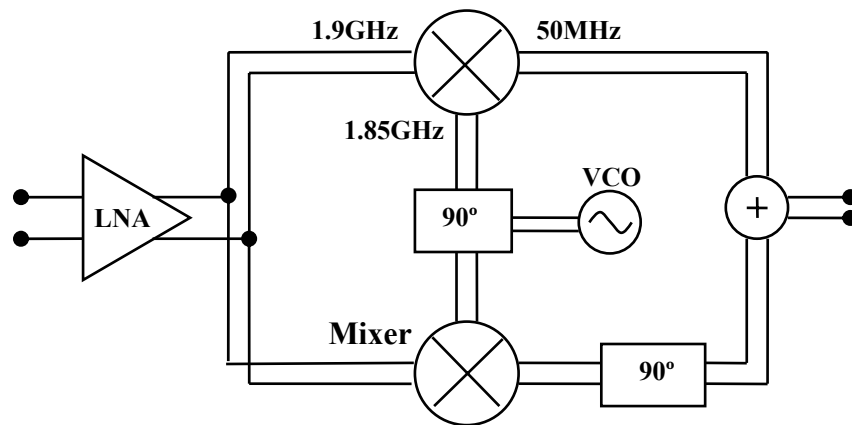

Figure 4: Hartley Architecture of Image Reject Mixer

4.2 Specifications

The specifications were previously calculated for the design of the overall project and for each sub-system block by the project supervisor, Dr. John Rogers. Table 2 lists the required specifications for the down converting mixer.

Table 2: Down Conversion Mixer Specifications

Parameter	Specification
Voltage Conversion Gain	$\geq$ 10dB
1dB Compression Point	$\geq$ -5.6dBm
Input Referred IP3	$\geq$ 5dBm
Single Sideband (SSB) Noise Figure	$\leq$ 10dB
Operating Current	$\leq$ 15mA
Supply Voltage	3.3v
Frequency	IF : 50MHz RF: 1.9GHz LO: 1.85GHz

4.3 Design Methodology

The double balanced Gilbert Cell was chosen to initiate the design process, it is known as an effective and well studied mixer topology. A schematical representation of the Gilbert mixer can be seen in Figure 5.
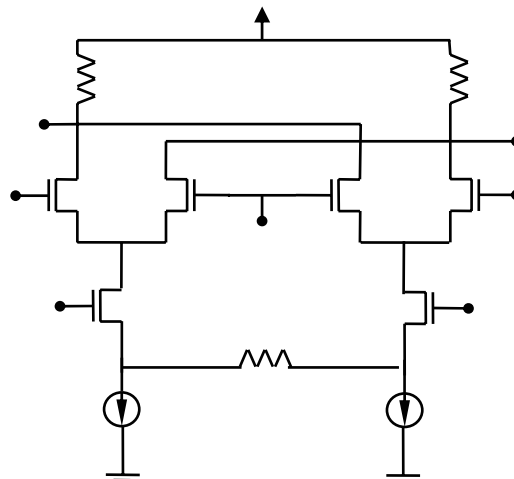

Figure 5: Standard Gilbert Cell

4.3.1 DC Biasing

The first stage of the design process was to properly bias the mixer such that each transistor component will function in the correct region of operation. Beginning from the lowest voltage in the circuit, V_{SS} (ground) we note that the current sink requires a minimum of approximately 0.4v for efficient operation, as will be discussed in subsequent sections. The RF transconductance stage (transistor M1), operates in the saturation region for optimum gain, therefore it is necessary that $V_{DS1} > V_{GS1} - V_T$. If the RF_{BIAS} is set to 1.4v, this will allow for reasonable RF AC input swing as well as ensuring transistor M1 remains in saturation at all times. Since $V_{D1}=V_{S3}\approx1.5v$, and transistor M3 should reach saturation for maximum gain, therefore $V_{DS3} > V_{GS3} - V_T$. After several simulations it was found that V_{G3} should be approximately 2.2v, this will ensure that transistor M3 can reach saturation and that the IF AC output signal swing will not interfere with the RF signal swing until higher power input levels are assumed. Finally, V_{D3} should be approximately 2.5v, allowing for (V_{DD}-V_{D3}) 0.8v voltage drop to be applied across the load resistor R_C. Figure 6 gives reference to a divided Gilbert mixer wherein transistor M3 experiences maximum current flow, I_{Bias2}.
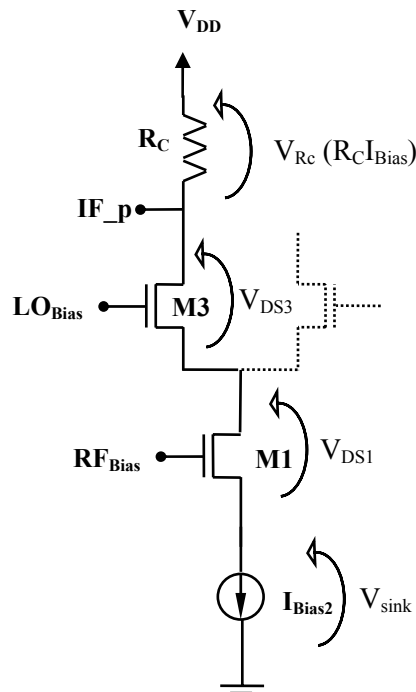

Figure 6: Biasing Mixer Voltages

4.3.2 Initial Simulation Trials

Upon initial simulation results of the Gilbert cell configuration, it was apparent that the specified design goals would not be achievable. The specified gain for the mixer was to be at least 10dB, however following several optimization attempts; the maximum achieved gain was approximately 5dB. It became necessary to choose a different circuit configuration which allowed for higher gain. A mixer topology which proclaims to allow for higher gain is known as a "Folded" Mixer; the reasons for its higher gain performance will be investigated and discussed in the following section of this report. As such, the remainder of this report will be dedicated to Folded Mixer design strategies.

4.4 Folded Mixer Design

The theory behind the Folded Mixer configuration as compared to that of a conventional Double-Balanced Mixer configuration (as discussed previously), remains for the most part unchanged. The most notable physical differences in circuit topology can be seen in Figure 7, here we see that the driver stage transistors (transconductance stage), are removed from the switching quad. The structure of the driver stage transistors now closely resembles that of a simple differential pair amplifier. Input RF current is amplified and fed into the switching quad network as in conventional Gilbert mixers. Ensuring that only AC current will flow into the switching quad, coupling capacitors C_C are used, the size of these capacitors will be limited by process restrictions and chip area. Driver stage load resistors R_{CC} are implemented such that input RF current will flow up into the switching quad with sufficient gain and that transistors M1 and M2 are properly biased. Degeneration resistor R_E will provide the overall mixer with improved linearity and stability during temperature fluctuations. The switching quad comprises of NMOS transistors M3, M4, M5 and M6, these transistors will oscillate (between on and off states) according to the input frequency of the LO. Load resistors R_C are used to convert mixed signal current into output IF voltage, the size of these resistors will influence the overall gain of the system and will be limited by remaining headroom voltage. Capacitors C_C will be implemented so that the output signal will be tuned to the output frequency, (the IF frequency). Both RF and LO input signals and the IF output signal are fully differential.
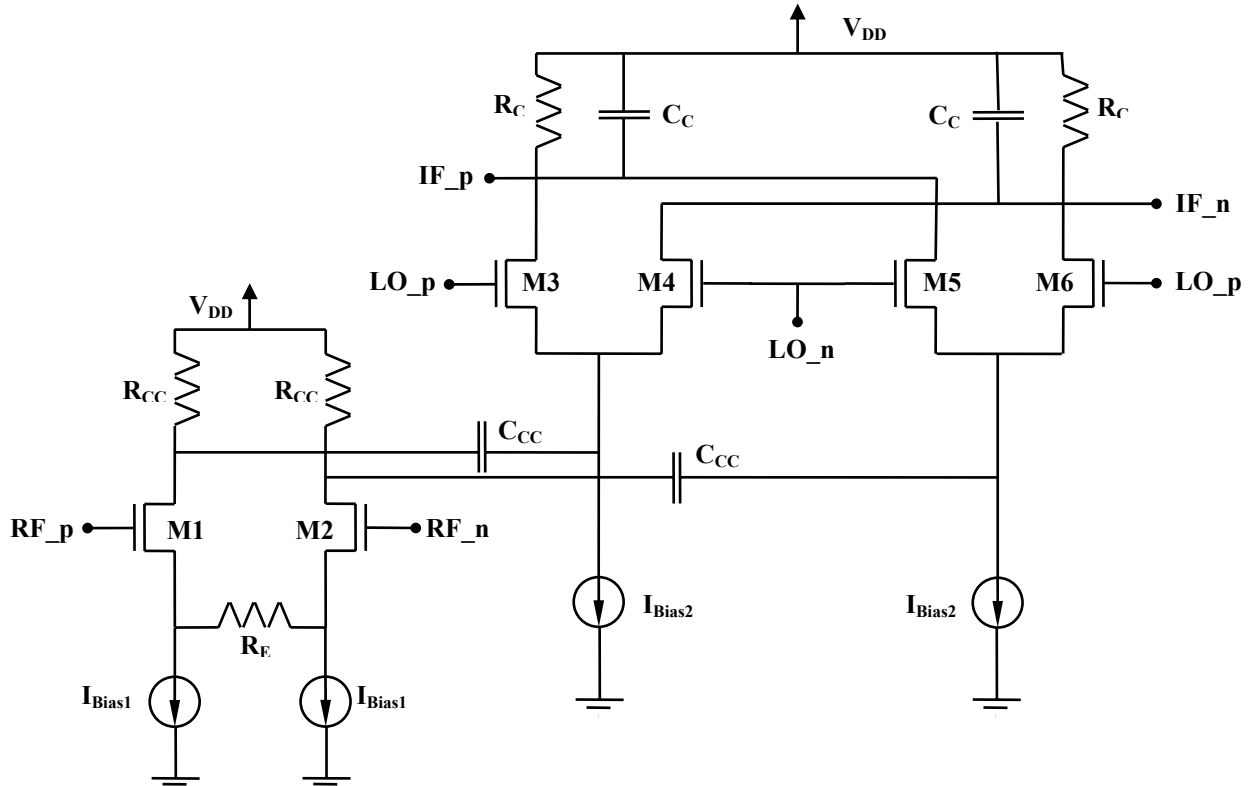
Figure 7: Folded Mixed Topology

The main advantage or attractiveness of the Folded Mixer design is attributed to the strong improvement in mixer gain. As previously discussed (§ 4.3.1), devices M3, M1 and the current sink device require a certain voltage drop across them such that they are able to function in the saturation region of operation, any remaining voltage (supply voltage less mixer operation voltage[1]) can be applied across the load resistor R_C. In the case of the Folded Mixer design, the mixer operation voltage is decreased by approximately 1.5v, this is because the driver stage is now separate from the switching quad and current sink transistors. This serves to alleviate headroom restrictions in that a larger voltage can now be applied across the load resistors R_C. By simply investigating Ohm's law V=I·R and noting that current remains fixed, it is apparent that an increase in voltage drop across resistor R_C will serve to increase the size of resistor R_C. Since the gain of the mixer is closely related to the output resistance, R_C, a larger load resistor will imply a higher gain.

---

[1] Voltage required to keep Driver, Switching and Current Sink transistors in saturation.

4.5 Design Procedure

The design procedure of the mixer is basically comprised of executing several simulations until a desired result or mixer performance was achieved. There are several factors which reflect mixer performance, such as gain, linearity, power and noise performance. Adjusting circuitry for the purpose of optimizing a particular performance parameter may serve to unintentionally degrade the performance of the other parameters. It is important to monitor all of the performance parameters throughout the design process.

The first stage in the design process was to approximate values for each circuit element in the mixer. The following discussion will outline how these approximations were achieved.

4.5.1 Transistor Operation

All transistors are to operate in the saturation region. For this requirement to be met, two expressions must be satisfied:

$$V_{GS} \geq V_{TH}$$
$$V_{DS} \geq V_{GS} - V_{TH}$$

Once these conditions have been satisfied it is possible to approximate the transistor behaviour in the saturation region through the following equation:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

The parameters which remain fixed in the above equation are μ_n, C_{ox}, L and V_{TH}. The parameters which can be adjusted for optimization are I_D, W and V_{GS}.

4.5.2 Transistor Biasing

A common practice in RFIC design is to ensure that the gate bias voltage relative to the source voltage V_{GS} is between 200mV and 400mV above the threshold voltage V_{TH}.

$$V_{GS} - V_{TH} \geq V_{safety}$$

where:

$$200mV \leq V_{safety} \leq 400mV$$

4.5.3 Gain

An approximation of the mixer gain is as follows:

$$A_v = \frac{1}{\left(\dfrac{1}{g_{m2}} + R_E\right)} \cdot \frac{4R_C}{\pi R_E}$$

This approximation is valid if the switching stage transistors are considered to act as perfect switches. There are several factors that affect the gain of the mixer. Since the gain is a strong function of R_C, one may consider increasing this parameter, in fact the added gain improvements achieved by increasing R_C is the main reason the Folded Mixer was chosen over the conventional Double-Balanced mixer design. One may also consider increasing the transconductance of the driver stage transistors, g_{m2}. Since g_{m2} is a function of I_{D1} and the driver stage overdrive voltage:

$$g_{m2} = \frac{2 \cdot I_{D1}}{\left(V_{GS} - V_{TH}\right)}$$

Increasing g_{m2} can be accomplished by increasing the transistor current I_{D1} or decreasing the overdrive voltage. Decreasing the degeneration transistor R_E may also serve to increase the overall gain, this will however have a degrading effect on the mixers linearity.

4.5.4 Linearity

A circuit will exhibit nonlinear characteristics when there is a variation in the small signal gain with respect to the input signal level. The resulting output signal will be distorted or compressed. There are three phenomena which affect linearity in the mixer circuit.

The first source of compression occurs at the driver stage. If the applied signal at the driver stage is greater than the maximum differential input (also known as overdriving) compression will take place. Linearity can be improved in this situation by decreasing the driver stage transistor ratio $(W/L)_{1,2}$, increasing the bias current I_{Bias1} and increasing R_E. Trade-offs to these corrections will serve to increased overdrive voltage (resulting in a decreased transconductance g_m and hence decreased gain), increased power dissipation and again decreased gain, respectively. [5]

The second source of compression occurs at the output load. If the output load resistor size R_C, is too large, the voltage drop V_{DS} across the switching transistors will decrease thus forcing the switching transistors out of saturation and into the triode region of operation ($V_{DS} < V_{GS} - V_T$). Reducing the size of the load resistors will move the DC output voltage to a higher level, this serves to reduce the gain as previously discussed. Reducing the bias current I_{Bias2}, will help solve this problem without severely affecting the gain. [5]

The third source of compression occurs at the driver stage drain voltage V_{D1}. As in the switching transistors, the driver transistors are required to operate in the saturation region of operation. The voltage across these transistors $V_{DS1,2}$ are set by the DC voltage level set by transistors R_{CC} (i.e. $V_{D1} = V_{DD} - I_{D1}R_{CC}$). Adverse affects include a reduction in gain. [5]

4.5.5 Noise Figure

Thermal noise and flicker noise are the two main sources of noise in most CMOS circuits. Thermal noise exists due to the randomness of electron behaviour in any conductor, in MOSFET technology the conducting component is the channel. Flicker noise occurs when charge carriers are trapped and released by interfering dangling bonds. Decreasing the size of the degeneration resistor will significantly improve the noise figure, however the linearity of the overall system will decrease.

Table 3 shows the final values chosen for each component in the mixer circuitry after optimization. Figure 8 shows the Folded Mixer topology with optimized component values.

Table 3: Final Component Values for Folded Mixer

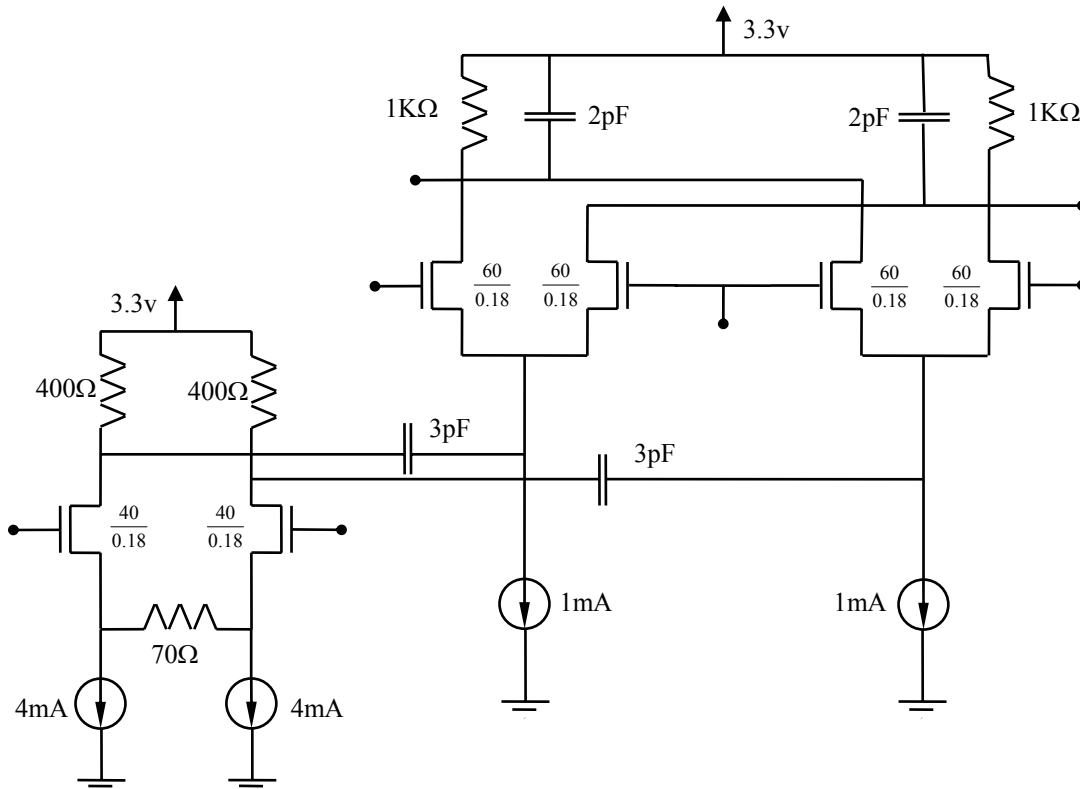| Component	Value
M1, M2	W/L = 40μ/0.18μ
M3, M4, M5, M6	W/L = 60μ/0.18μ
R_{CC}	400Ω
R_C	1KΩ
R_E	70Ω
C_{CC}	3pF
C_C	2pF
I_{Bias1}	4mA
I_{Bias2}	1mA

Figure 8: Folded Mixer Topology With Optimized Component Values

4.6 Discussion

In order to drive the expected 2KΩ load without degrading the performance of the mixer, an output buffer was implemented. The source follower is a common configuration and was implemented in the mixer design. The source follower will allow the gain to remain consistent with the expected mixer gain while lowering the mixer's output resistance. Figure 9 illustrates the configuration and sizing used for the output buffer.
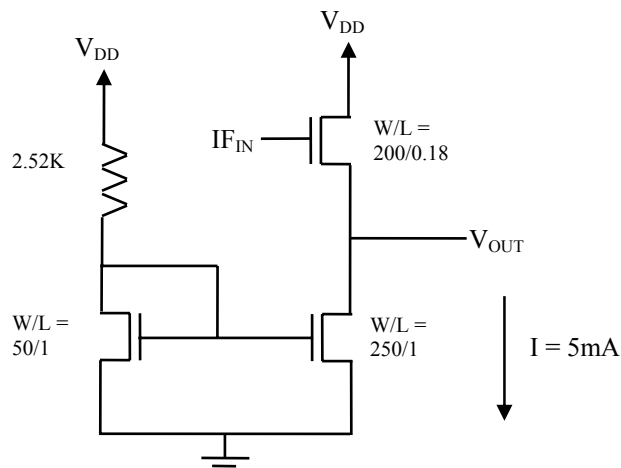

Figure 9: Output Buffer Configuration

Another modification which would improve mixer performance would be to change the load resistors R_C to active loads such as high impedance PMOS transistors. This will allow even higher gain without using up too much headroom and allows for smaller on chip space requirements as compared to a resistor.

5.0 Simulation

5.1 Simulation Results

All simulations were done using Cadence Spectre (version 4.4.6); the model file used to model the behaviour of NMOS transistors in the 0.18μ process was labeled "cmosp18" and was provided by the Canadian Microelectronic Corporation (CMC).

Table 4: Simulation Input Variables

LO Frequency	1.85GHz
LO Power	0dBm
LO Input Impedance	100Ω
RF Frequency	1.9GHz
RF Power	-16dBm
RF Input Impedance	100Ω

Mixing the LO frequency with the RF frequency results in a desired down-converted frequency at 50MHz and an undesired up-conversion frequency of 3.75GHz accompanied by undesired intermodulation and third order harmonics which span much of the frequency spectrum.

5.1.1 DC Analysis

A DC simulation is used to verify the operating and node voltages of the circuit. It also serves to verify bias voltages and currents of each transistor within the mixer. The DC analysis was used to ensure that all transistors were operating in the expected region of operation prior to the application of AC input signals LO and RF. The DC analysis also provides information regarding transistor characteristics such as g_m, g_{ds}, V_{th}, V_{DS} and V_{DSsat}. This information can prove to be helpful when optimizing circuit performance. The DC analysis of the Folded Mixer is illustrated in Figure 10 and Figure 11.
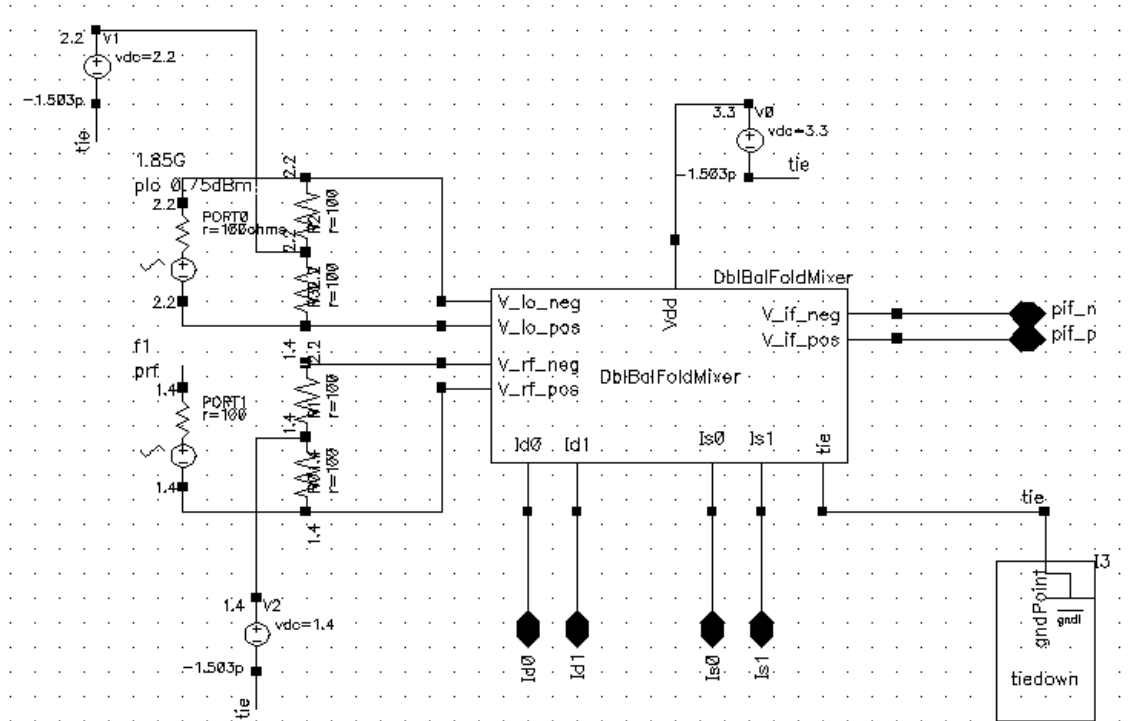
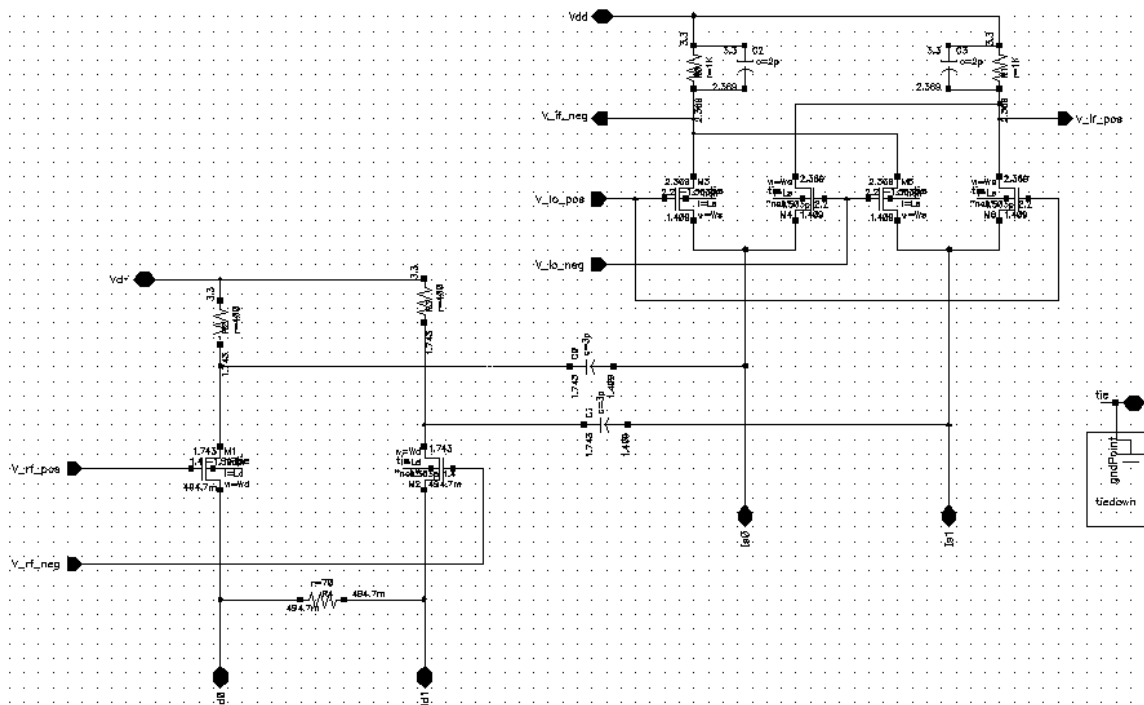**Figure 10: Folded Mixer Testbench DC Analysis**

Figure 11: Folded Mixer Core DC Analysis

5.1.2 Transient Analysis

The transient analysis displays the AC signals in the time domain. Figure 12 shows the IF output signal which comprises of both desired 50MHz, and undesired 3.75GHz signals. A rough approximation of the mixers gain can be obtained as follows:

$$Gain(dB) = 20\log\left(\frac{V_{out,pp}(IF)}{V_{in,pp}(RF)}\right) = 20\log\left(\frac{2(310.7)mV}{2(94.4)mV}\right) = 10.34dB$$

The output frequency IF, is verified for correctness:

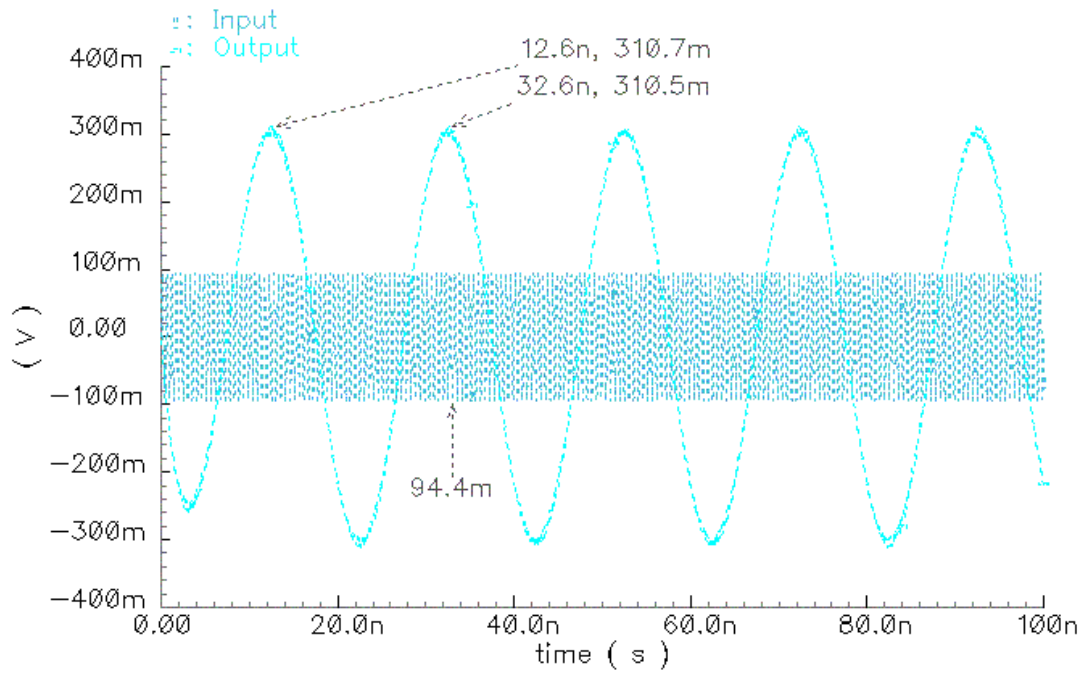$$Frequency = (period)^{-1} = (32.6n - 12.6n)^{-1} = 50MHz$$

Figure 12: AC Analysis of IF Output Signal

5.1.3 Periodic Steady State (PSS) Analysis

The PSS analysis is a large signal analysis which directly computes the periodic steady state response of a circuit. The PSS simulations are computed by first performing a transient analysis until the circuit has settled, the simulator then performs a Fourier analysis on one period of the transient signal, thus generating a frequency spectrum of that signal. Figure 13 shows a frequency spectrum of the output signal, the plot clearly indicates the presence of the 50MHz down-converted signal and the 3.75GHz up-converted signal. The PSS analysis function also provides the designer with signal output power levels in dB's. The desired IF output frequency yields a voltage conversion gain of 10.17dB, while the unwanted up-converted signal yields -22.07dB. Relative to the IF signal the up-converted signal experiences 32.24dB of attenuation, this is largely due to the implementation of the tuning capacitors C_C.
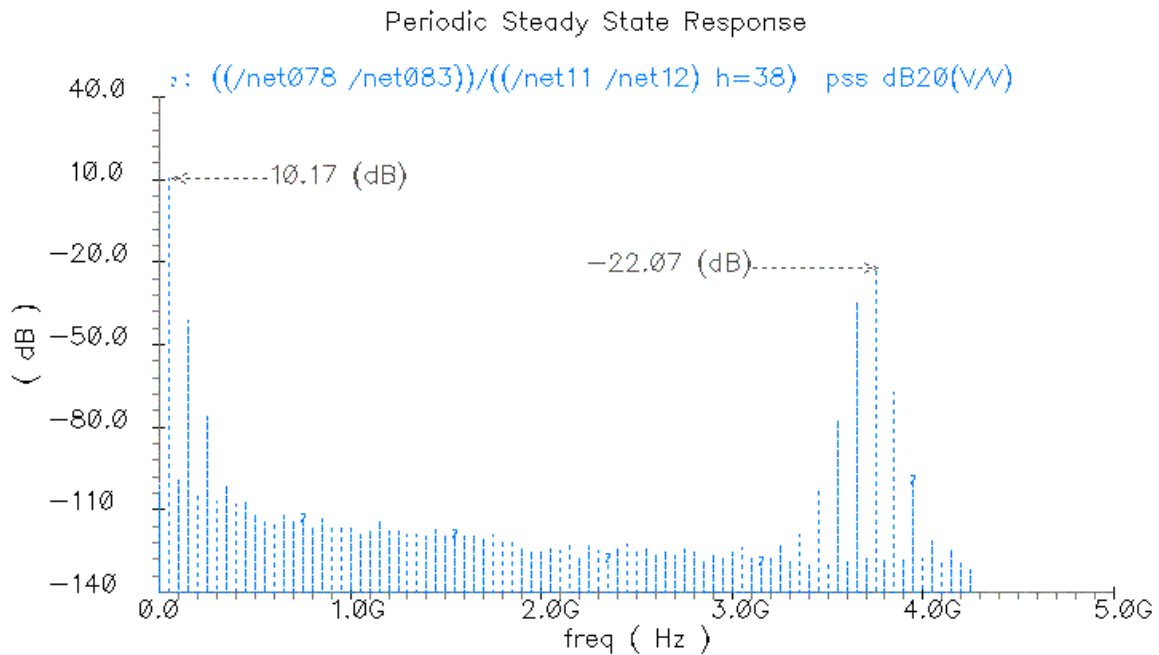

Figure 13: DFT, Output Frequency Spectrum

5.1.3 1dB Compression Point

In order to determine the 1dB compression point of the mixer, a swept periodic steady state response (SPSS) analysis is used. The SPSS simulations are similar to that of PSS simulations, however in SPSS analysis a variable, namely RF input power, is swept from -25dB to 0dB as shown in Figure 14 below. This analysis is used to determine the 1dB compression point. The figure also shows that the 1dB compression point or P1dB occurs when the mixer receives an input of -5.478dBm.
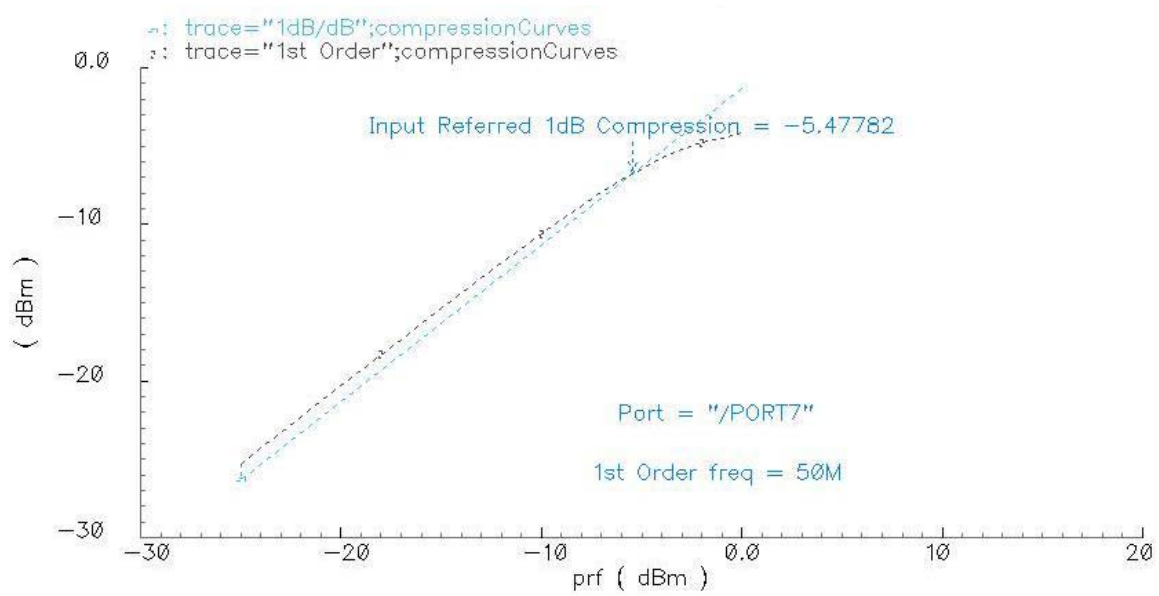

Figure 14: P1dB Compression Point

5.1.4 IIP3 Intercept Point

The SPSS analysis is used in conjunction with a periodic AC analysis do determine the third order intermodulation point. These simulations are combined and used to analyze two small signal input tones at the RF input. These tones occur at the expected input frequency of 1.9GHz and at an interfering signal (a neighbouring channel frequency) of 1.91GHz. These two signals will mix with the LO to produce second order (IM2) effects at 50MHz and 60MHz respectively. The third order intermodulation (IM3) products will appear at 40MHz and 70MHz. A common approximation used to calculate the IP3 point is as follows:

$$IIP3 = (P1dB + 9.6dB) = (-5.4778 + 9.6) = 4.122dB$$

Table 5: PAC and PSS Frequencies

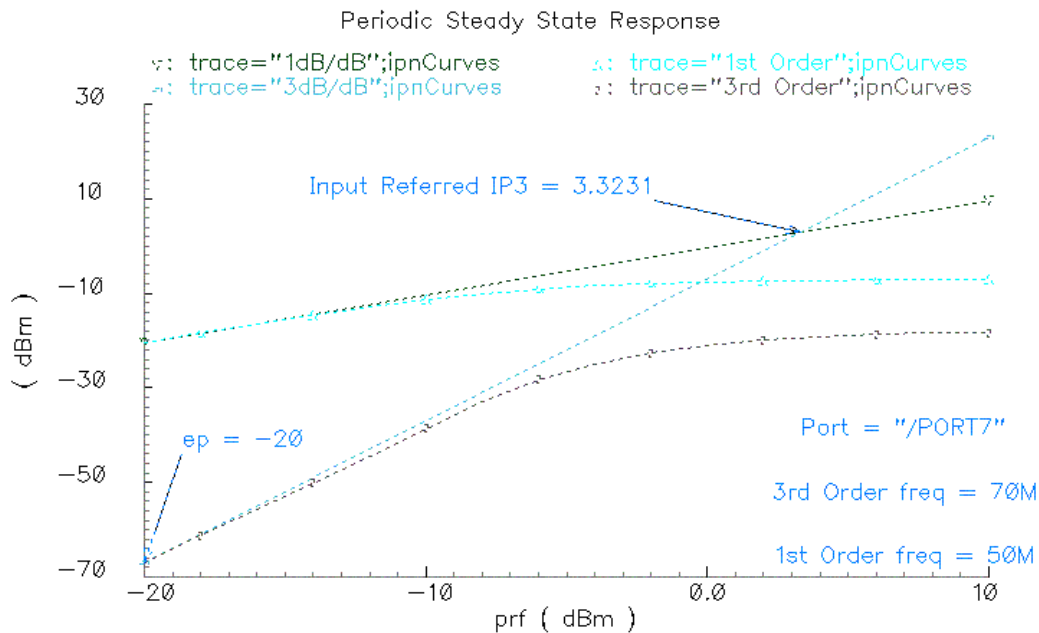| Port	Frequency	
RF	Desired	1.90GHz
	Interferer	1.91GHz
LO		1.85GHz
IF	IM2	50MHz
		60MHz
IF	IM3	40MHz
		70MHz

Figure 15: IIP3 Intercept Point

5.1.5 Pnoise

The single sideband noise figure (SSB NF) of the mixer was found by using the SPSS analysis followed by a Periodic Noise (Pnoise) analysis. The Pnoise analysis computes the total noise contribution to the input signal from the circuit. Noise is contributed to the mixer from components such as resistors and transistors, input and output sources and frequency translation. As seen in Figure 16, the single sideband noise figure is 15.05dB.
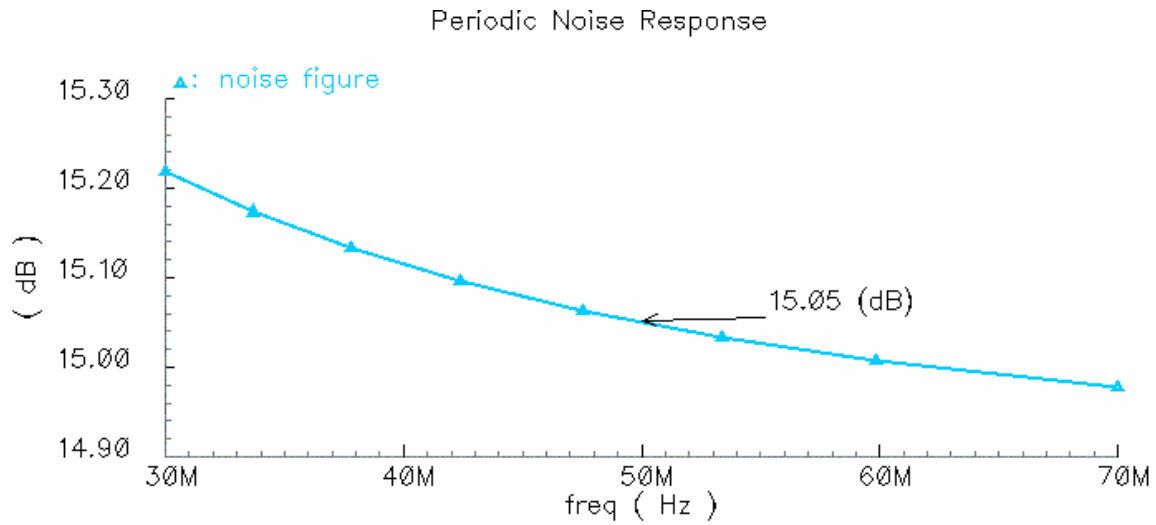

Figure 16: Noise Figure

5.2 Mixer Performance Summary

Table 6 below list the simulated results as compared to the specification requirements given previously in Table 2 of section 4.2.

Table 6: Mixer Performance Summary

Performance Measure	IC Tuner Specification	Simulation Results	Deduction
Voltage Conversion Gain	$\geq$ 10dB	10.17 dB	Pass
1dB Compression Point	$\geq$ -5.6dBm	-5.48 dBm	Pass
IP3 Point	-------	3.323 dBm	Pass
Noise Figure	$\leq$ 10dB	15.05 dB	Acceptable
Power Consumption	$\leq$ 15mA	10mA	Pass

All of the mixer's performance characteristics are met apart from the noise figure parameter. After consultation with the project supervisor it was concluded that the simulated noise figure was an acceptable value given the nature of the design. The noise figure is expected to be significantly reduced once the preceding LNA is implemented.

6.0 Layout

The layout design for this project was completed using Cadence Virtuoso Design Editor Environment in 0.18μ technology. The purpose of the layout stage is to provide the chip manufacturer with a physical map depicting the dimensions and placement of all the electrical components encompassed in the mixer design. The layout tool is also helpful in realizing the physical behaviour of the mixer, just as the schematic editor can approximate component behaviour through simulation, the layout tool can further approximate physical behaviours (i.e. parasitics) through simulation.

All of the components in the mixer are symmetric with respect to other components in the same stage of the mixer, i.e. switching LO quad, differential RF pair, current mirrors and load resistors. Therefore in order to facilitate design repetition, cells were used to design layout for a particular stage. Once all of the components were individually designed, the overall mixer was collectively assembled using the previously designed cells. Modular design helps the designer optimize each stage of the design without having to redesign the entire mixer circuit.

Virtuoso is also equipped with a DRC (design rule check) operation, this function checks for design violations, ensuring that manufacturing capabilities match the proposed layout design.

6.1 Design Issues

6.1.1 Space

The final goal of the project is to be able to physically implement the cable tuner on a single IC chip. As of yet the physical size of the chip is undetermined, therefore the area in which the layout will be placed is also undetermined. However, the mixer will be implemented in a compact manner such that chip minimization can be achieved. As in the schematical representation of the mixer, the layout will consist of two 3pF coupling capacitors as well as two 2pF tuning capacitors, it is important to note that the physical size of these four capacitors will consume over 60% of the design area.

6.1.2 Resistivity

Since the transistor size ratios are quite large (i.e. switching stage transistors where W/L = 60μ/0.18μ) the relative gate length will be over 300 times its width, thus inducing a notable gate and source/drain trace resistance. In order to minimize gate resistance, multiple parallel transistors, or multifinger design was implemented such that the total length per gate finger relative to gate width is minimized, thus reducing gate resistance. Source/drain connections also benefit from mulitifinger design for the same reasons. Trace resistance is reduced by adding several via contacts along the active regions, ensuring evenly distributed transistor actuation and safeguard connections in the case that a via connection should fail. Trace resistance is further reduced by routing interconnections with 45-degree angles rather than 90-degrees as suggested by TSMC. [6]

6.1.3 Symmetry

It is important that the components in the differential pair, as well as the rest of the circuit, remain symmetrical such that amplitude and phase mismatch as well as LO feedthrough and common mode noise are minimized. The layout was designed about a vertical axis in which each component was perfectly mirrored, thus improving component symmetry. Figure 17 illustrates the completed mixer design which is perfectly symmetric about the vertical axis.

6.1.4 Process Variations

Unfortunately all processes will introduce material inconsistencies throughout the chip wafer, such as oxide thickness and compound purity levels. These errors can be reduced by using layout techniques called interdigitization and common-centroid configuration. In either case transistor gates are interleaved amongst one another so that process variations will equally affect the performance of the two transistors.
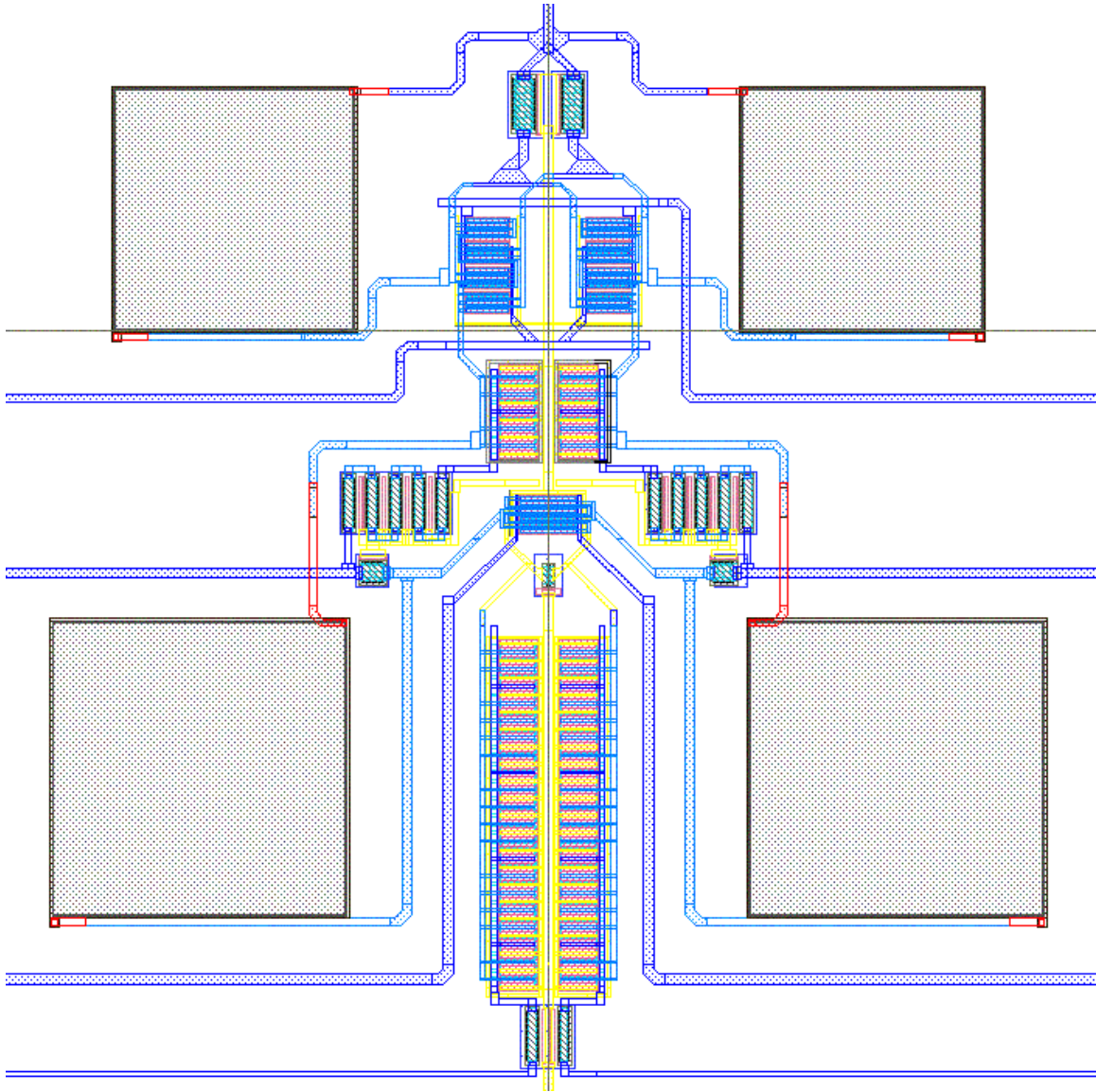
Figure 17: Complete Mixer Layout Top View

6.2 Mixer Core

6.2.1 Driver Stage

As shown in Figure 18, the driver stage experiences symmetry about the vertical axis, the construction also employs interdigitization. Both 40µ/0.18µ transistors have 4 gate fingers, each 10µm long.
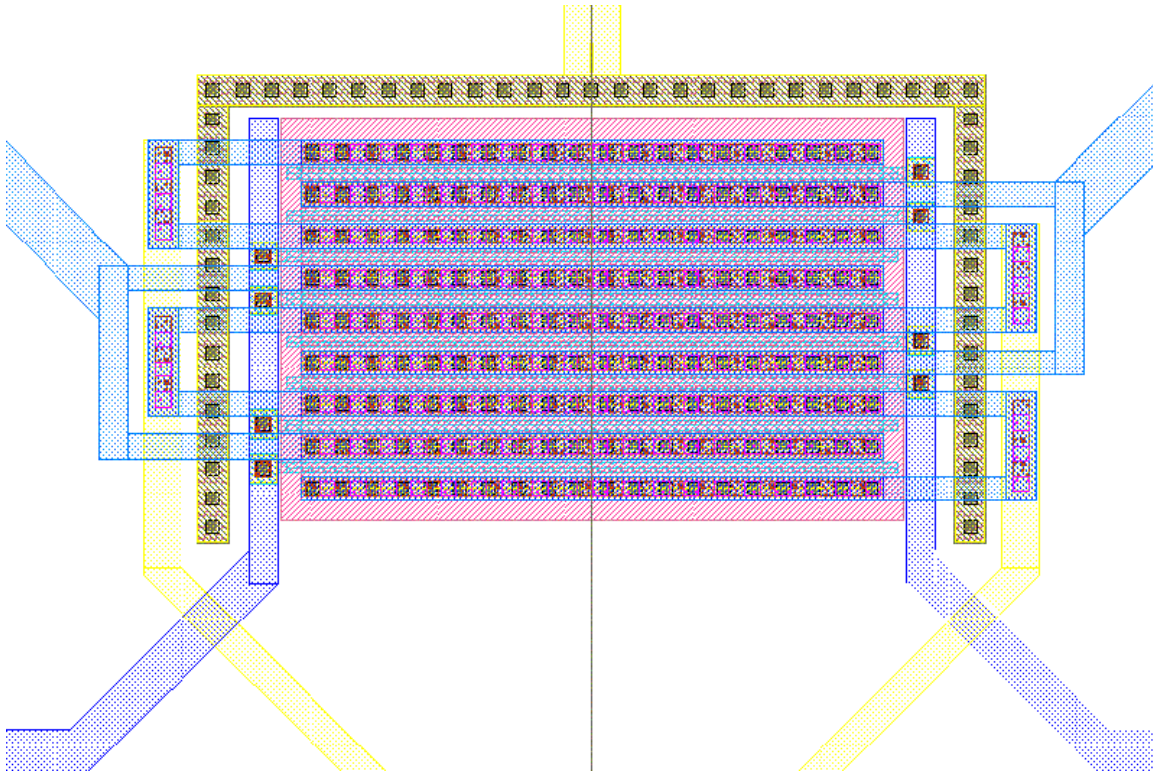

Figure 18: Driver Stage Layout View

6.2.2 Switching Stage

The switching quad transistors, Figure 19, are each 60μ/0.18μ. These transistors are interdigitated however not shared as in the driver stage. This technique minimizes interface between the pair during on/off switching. Each transistor is composed of 8 fingers, all 7.5μm long.
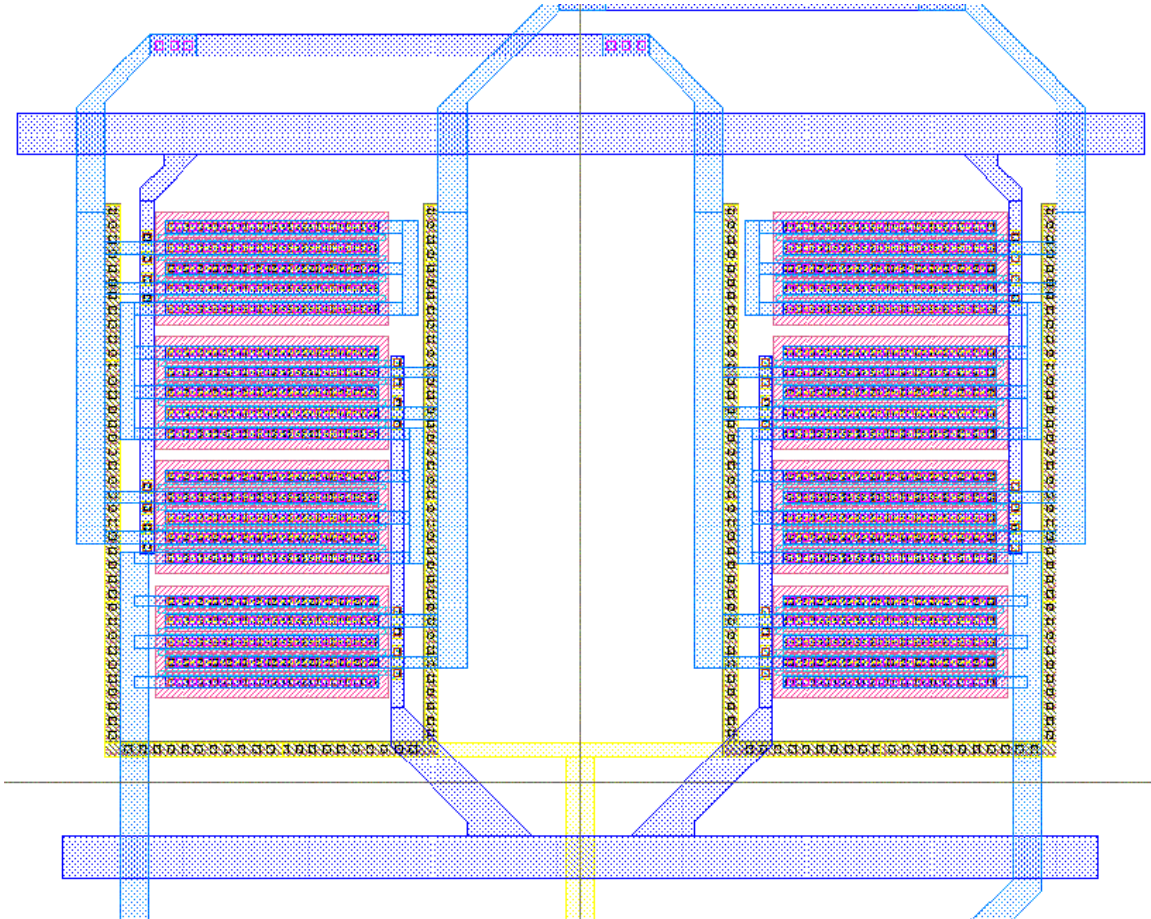

Figure 19: Switching Stage Layout View

6.2.5 Load and Bias Resistors

The resistors featured in Figure 20 are used to bias the 4mA current sinks. They are composed of a high resistance poly layer PO and resistance protection oxide RPO. These layers are then enclosed in an n-well to reduce noise emerging from the substrate. The resistance values are approximately 2.53KΩ.
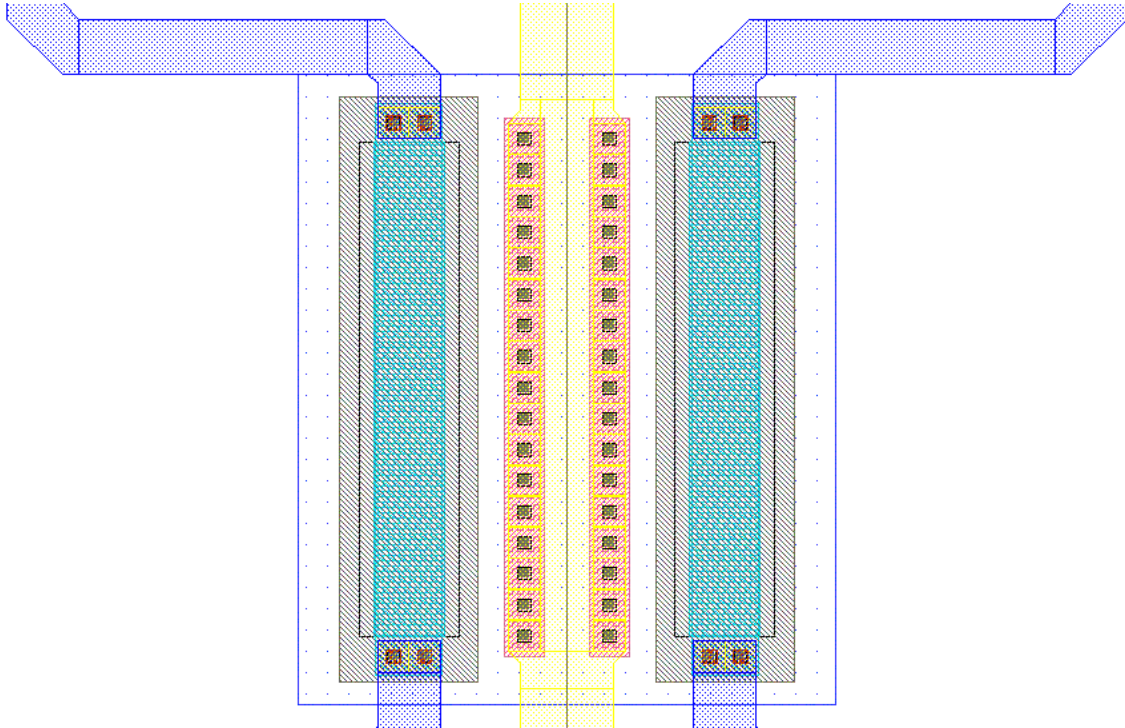

Figure 20: 2.53KΩ Bias Resistors

The resistors featured in Figure 21 are used to bias the 1mA current sinks. Again, they are composed of a high resistance poly layer PO and resistance protection oxide RPO enclosed in an n-well. The resistance values are approximately 11KΩ. They were constructed using 5 repetitions of 2.2KΩ resistors configured in series.
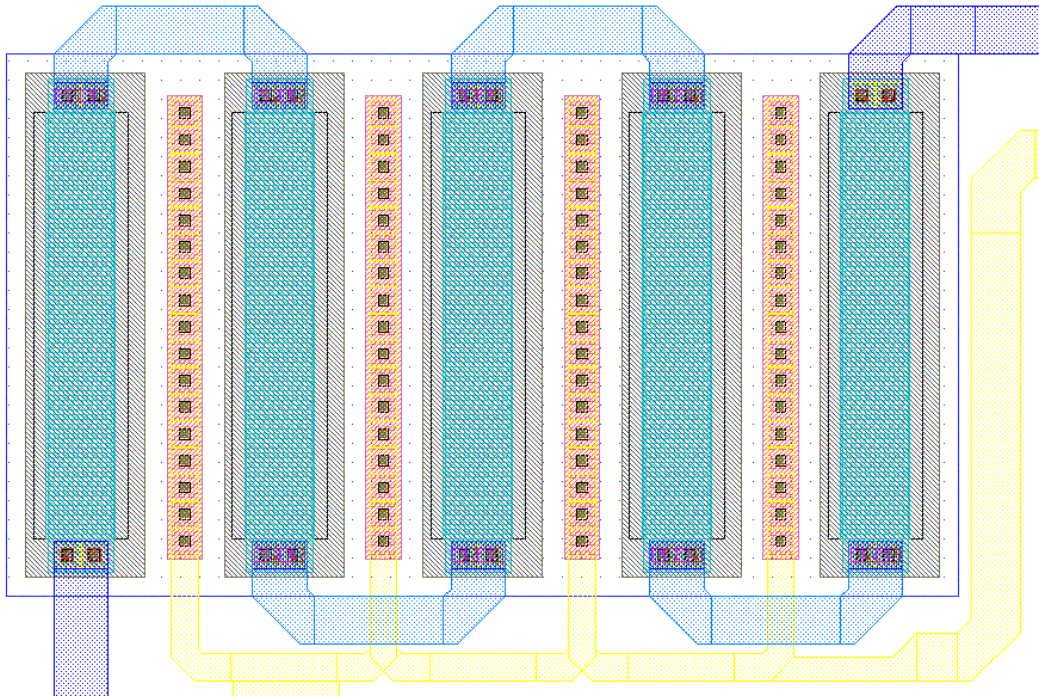

Figure 21: 11KΩ Bias Resistor

6.2.6 Coupling and Tune Capacitors

The capacitors used for this project originated from pre-designed examples found in the cmosp18 library file. In contrast to the other devices, little effort was required to implement the capacitors.
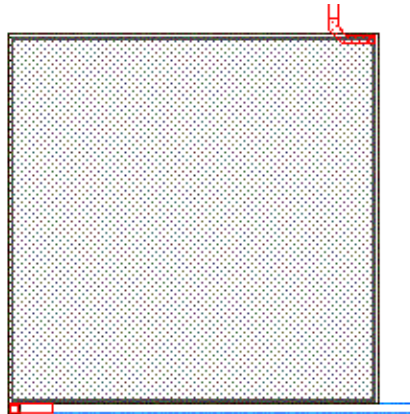

Figure 22: 3pF Capacitor

7.0 Support Circuitry

7.1 Current Sink

The circuits used to sink current in the mixer were NMOS current mirrors. Two 4mA current sinks were required for the driver stage and two currents sinks were required for the switching stage. Figure 23 shows an encapsulated view of both current sinks as they appeared in the simulation environment.
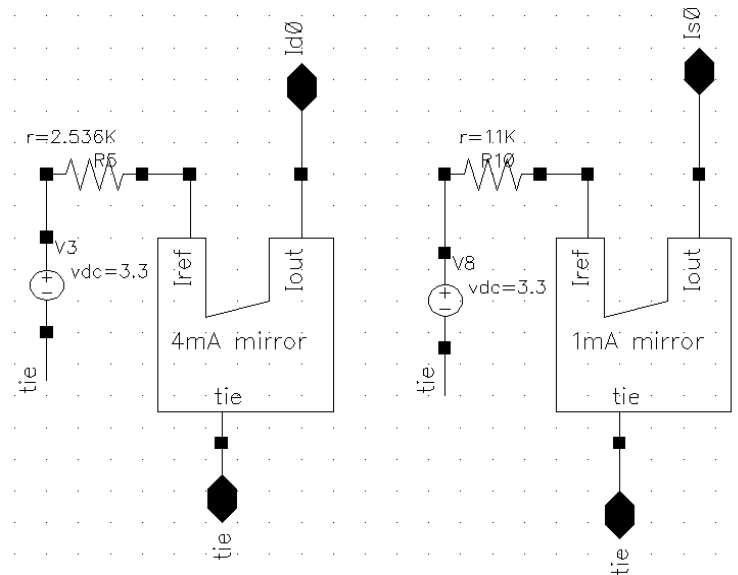

Figure 23: Top Level View of 4mA and 1mA Current Sinks

The transistor length parameters used in the current mirrors were chosen to be 1μm, approximately 5 times the minimum process length. This will ensure that the channel length modulation coefficient λ, will be minimized and thus optimizing the output resistance of the current mirrors. A higher output resistance will facilitate current stability upon changes in V_{DS}.

7.1.1 1mA Current Sink

The 1mA current mirror schematic and layout diagrams are shown in Figures 24 and 25 respectively. The reference current is a quarter of the output current, this was established using W/L ratios of 12.5µ/1µ to 50µ/1µ. The layout was designed using common-centroid technique to counter effects of linear gradients. There are 10 fingers in total, each 6.25µm long.
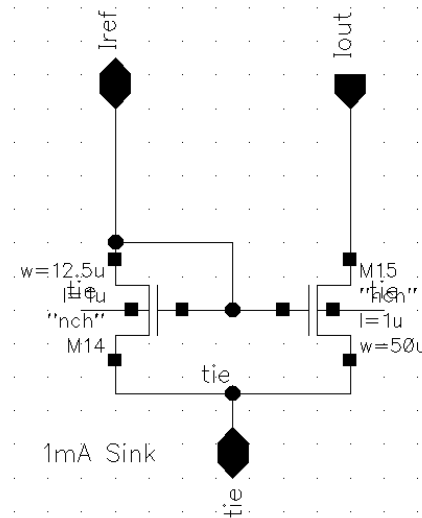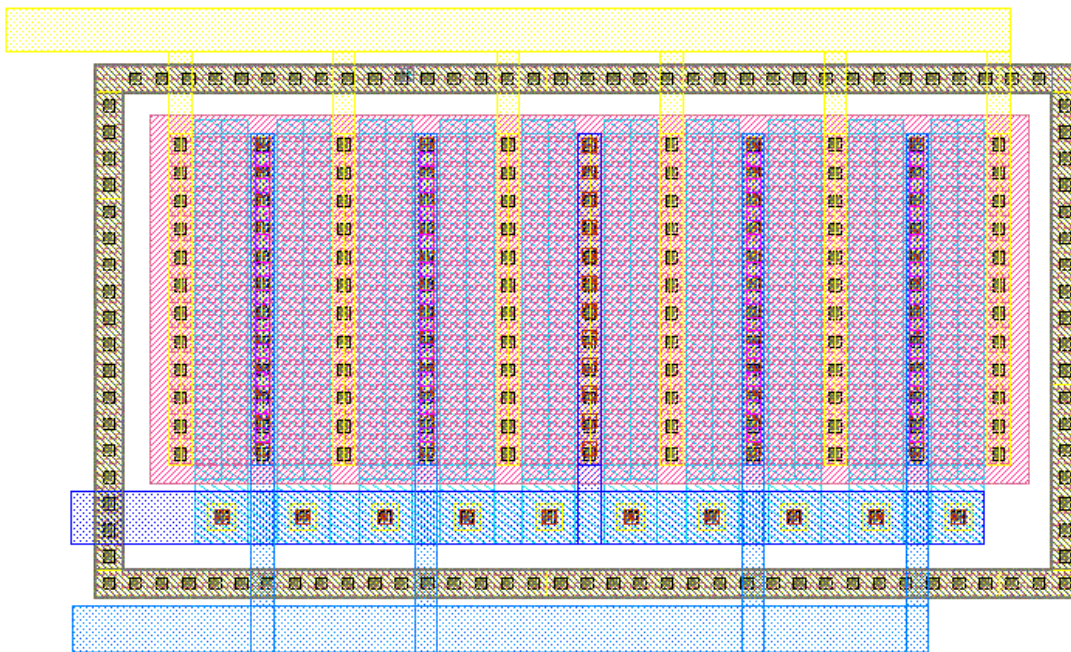

Figure 24: 1mA Current Sink Schematic View

Figure 25: 1mA Current Sink Layout View

7.1.2 Driver Stage Current Sink, 4mA

The 1mA current mirror schematic and layout diagrams are shown in Figures 26 and 27 respectively. The reference current is a quarter of the output current, this was established using W/L ratios of 50μ/1μ to 200μ/1μ. (Note: in Figure 23, the output transistor has a multiplicity of 2) Again, the layout was designed using common-centroid technique to counter effects of linear gradients. There are 40 fingers in total, each 6.25μm long, and the appearance of this current sink as compared to that of the 1mA current sink establishes a much more rectangular form. This is because the design rules for this process state that the body contact must be within 5μm of any active region, in this case the source and drain regions.
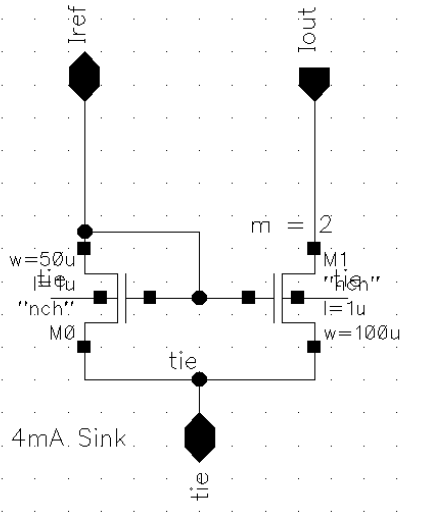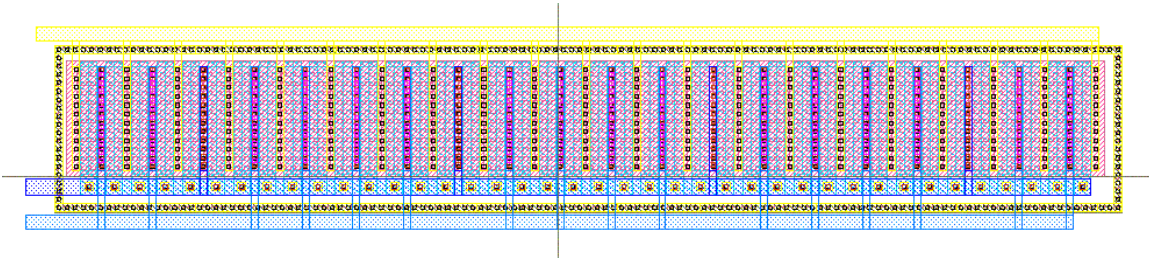

Figure 26: 4mA Current Sink Schematic View

Figure 27: 4mA Current Sink Layout View

8.0 Future Work

Although a great deal of the effort required for completion of the IR mixer stage has been accomplished, some remaining tasks must be accomplished such that the proposed IC Tuner Chip becomes realizable.

The Folded Mixer design stage has essentially been completed aside from the layout of the output buffer. Once the layout of the output buffer has been integrated into the Folded Mixer design, an Extraction simulation will be performed on the entire circuit. This will allow the simulator to model capacitive parasitics in the circuit due to trace overlaps. A Layout versus Schematic (LVS) check can then be executed. This verification routine compares the circuit layout with the schematical design, and will notify the designer if they do not match.

After completing the Extraction and LVS simulations, the Folded Mixer will then pass through all of the performance simulations described in section 5.0 of this document. This will provide the designer with a more accurate representation of the mixer's performance after the layout stage has been completed. These results will be compared with the specification requirements as in section 5.2 to ensure that the mixer's characteristics meet or exceed the requirements.

The Folded Mixer will then be combined with the other stages designed by the project group members to form a completed IC Tuner Chip as anticipated. The competed chip may then experience a Top-Level simulation prior to Tape-Out.

9.0 Conclusion

Mixers are an essential component in most modern telecommunication circuits because they provide integrated communication systems with the necessary frequency translation required for data transmission. The Folded Mixer designed in the project was intended as a down-conversion mixer for use in a Cable Tuner receiver.

The Folded Mixer was designed and tuned with the Cadence Design Environment using $0.18\mu m$ CMOS technology, the model files were provided by CMC. After optimizing the devices in the Folded Mixer design, simulated results were compared to the specification requirements, ensuring all performance characteristics were met. The mixer then entered the layout stage wherein the physical structure of the circuit was realized.

Designing the mixer was the most challenging portion of this project. Thorough understanding of CMOS technology was an essential learning component of this project. Predicting the effects of changes in device properties drastically reduced the optimization period. It was quite helpful to begin the design using the convention Gilbert topology. This allowed for easier understanding of mixer theory and allowed for a smooth progression towards the Folded Mixer design.

Learning how to use the Spectre simulation tool was a collaborated effort put forth by all group members, thankfully after undertaking several tutorials while attending Spacebridge Semiconductor Co., most functions and tools were well-known prior to the projects commencement.

The layout stage was quite time consuming and tiresome however great care went into ensuring proper design. (i.e. minimizing area , capacitance and resistance)

The design of a Folded Mixer was an excellent learning experience. This project was a quite relevant to projects undertaken by RFIC design companies located in the Ottawa area. The Folded Mixer design is also relevant to mixers using a 1.8v power source, as headroom is increasingly becoming a design issue.

10.0 References

[1] John W. M. Rogers, Brian Robar, Walt Bax, Zhan F. Zhou, Sivakumar Kanesapillai, Stefan Fulga, Mike Toner, and David Rahn "A Completely Integrated Cable Tuner", SiGe Semiconductor 2001. pp. 1-4.

[2] Plett, Dr. Calvin. "97.455 Telecommunications Theory", 2000. pp. 1-15, 34-40.

[3] Lee, Thomas H. "the Design of CMOS Radio Frequency Circuits". Cambridge University Press, Cambridge, United Kingdom, 1999. pp. 309-313, 319-321, 324.

[4] Razavi, Behzad. "RF Microelectronics". Prentice Hall, Upper Saddle River. N.J. 1998. pp. 38-41, 48-50, 131-132, 138-143, 182-187.

[5] John W. M. Rogers, Calvin Plett "Chapter 7, Mixers", 2002. pp. 44-62.

[6] TSMC, Taiwan Semiconductor Manufacturing Co., "TSMC 0.18µ Mixed Signal/RF 1p6M Salicide 1.8V/3.3V Design Rule", Document No. TA-10A9-4001.