**ELEC 5705 RF System Design: Assignment #7**

Due April 24th, 2020

For this assignment you must design an ADPLL to generate the LO for a radio.

For the assignment you should build a loop as follows:



You should build all components out of behavioral blocks (as a suggestion use Simulink).

1. To start demonstrate a loop with a loop bandwidth to 150kHz,  = 0.707, Fref = 40MHz and FDCO = 4GHz.
2. Use a simple integer TDC in this loop.
3. Determine the spur levels at the output of the DCO when the loop is settled for a non-integer division ratio of your choice.
4. How much would the spur performance have to be improved to meet your specifications in either assignment #4 or #6?