

97.497 Final Project Report:

**Design of a Broadband Low-Noise Amplifier
For Use in a Cable Tuner**

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ABSTRACT

The need for cable tuners is growing significantly due to the requirement for faster and improved communication systems such as high-speed Internet access and cable television. The low-noise amplifier (LNA) is one of the major components in a cable tuner system.

This report attempts to explain the design of a low-noise-amplifier according to specifications. Using 0.18 μm technology to build the circuit and Cadence software to simulate its operation, the performance of the LNA was optimized through the use of different circuit topologies and components. Based on the results obtained from simulation, the components were varied and sized to reach the desired results. The other aspect of the design process that was explored was layout to assess the impact of physical structure on the operation of the LNA. To execute this task, the Cadence layout tool was used.

To a large extent, the objectives were met, thereby satisfying the requirements of the project. However, further study is proposed to explore the utilization of this technology in other applications.

1.0 INTRODUCTION

The focus of this project is the design of a broadband low-noise amplifier (LNA) to be used in a CMOS cable tuner. The LNA is designed to meet the specifications provided by Professor John Rogers.

The report has been divided into sections as follows: Objectives, Cable Tuner Overview, Design Methodology, Simulation Results, Layout, Conclusions, and Recommendations. A brief summary of the contents of each section is given below.

The Objectives section presents the overall goals, which were determined at the commencement of the project.

In the Overview section, the complete cable tuner is explained, along with the various circuit blocks from which it is built.

The Design Methodology section discusses the methods used to build the LNA, the specifications for the design, and the selection of the appropriate circuit technology. It also discusses the LNA circuit topology and gives detailed reasoning for choosing circuit configurations and components. The last sub-section of the Design Methodology deals with the sizing of all LNA transistors and components once the circuit topology was completed, taking into account the gain, input impedance, noise, and linearity requirements.

Simulation results are discussed in the fifth section of the report. Four different analyses were conducted and the results of each of them are compared to the theoretical expectations.

The Layout section deals with the on-chip layout design of the LNA. A discussion of the methods and tools used to complete this task is provided, as well as a description of the problems that were encountered at this stage of the design work.

The Conclusions section recapitulates the work that has been accomplished on the project and compares this work to the goals that were previously established.

Finally, in the Recommendations section, methods for improving the simulation results and suggestions for other applications of the LNA are offered.

2.0 OBJECTIVES

The following five objectives were established at the outset of the project:

- i) To develop a circuit topology and to size all circuit components to meet specifications; to build the LNA using 0.18 μm CMOS technology
- ii) To gain experience working with Cadence software and the various types of analysis, including scattering-parameter and periodic steady-state analysis
- iii) To simulate the LNA operation in Cadence to generate gain, input impedance, noise, and linearity results
- iv) To learn about the circuit design and operation of other cable tuner components such as mixers, and selected circuits of a frequency synthesizer such as the voltage-controlled oscillator and the phase detector
- v) To work collaboratively with an engineering design team, where each member is responsible for one aspect of the project

3.0 CABLE TUNER OVERVIEW

The cable tuner is an application of RFIC design that is in very high demand today because it can be used for delivering cable television and high-speed Internet access. As a result of the Internet becoming a primary medium for delivering and receiving information, the need for cable tuners has increased significantly. In order to meet the demands of consumers, the cable tuner must be designed such that it can handle many input channel signals simultaneously while consuming as little power as possible.

The cable tuner has been designed using CMOS technology to operate in a frequency range of 50 to 850 MHz. A two-stage design has been selected, with each stage containing various RFIC blocks such as broadband low-noise amplifiers, mixers, filters, and frequency synthesizers. The frequency synthesizer consists of several different circuits including a phase detector, voltage-controlled oscillator, and charge pump. The individual circuit blocks must be designed properly for the complete cable tuner to operate correctly. A schematic of the overall cable tuner can be seen in Figure 3.1. For this project, each member of the team has been assigned the design of a particular circuit block.

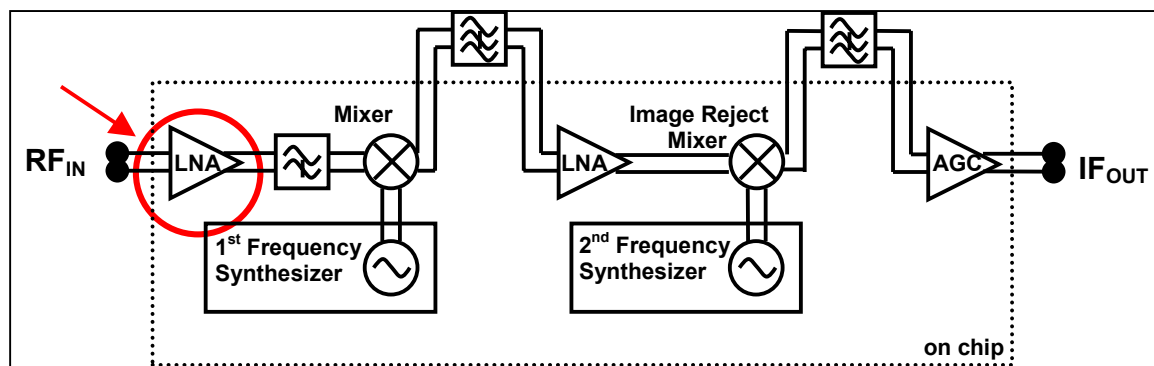


Figure 3.0 Overall Cable Tuner Design

As the first block of the tuner, the low-noise amplifier (LNA) must amplify the input signals, while adding as little noise as possible to the system. Once they have been amplified by

the LNA, the input RF signals are fed into the first-stage mixer, along with another signal, which is generated by a local oscillator (LO). The local oscillator signal ranges between 1.95 and 2.75 GHz. The RF and LO signals are then mixed together and up-converted to an Intermediate Frequency (IF) of 1.9 GHz.

At this point, the signals at IF are fed into the second stage of the cable tuner, which consists of a second LNA and a Down-Converting Image Reject (IR) Mixer. After further amplification by the second-stage LNA, the signals are fed into the IR Mixer, along with the 1.855 GHz signal of a second local oscillator and down-converted to an IF frequency of 45 MHz. In addition to down-converting the signals, the IR mixer gets rid of unwanted image signals that are present in the system.

The oscillators located in both the first and second stages are part of two frequency synthesizers present in the cable tuner receive block. In addition to the voltage-controlled oscillator, the frequency synthesizer consists of a phase detector and charge pump.

To start, the phase detector compares the phase and frequency of the input signals with that of the Voltage-Controlled Oscillator (VCO) and generates an error voltage. This error voltage is filtered and applied to the VCO as a control voltage. The control voltage forces the VCO frequency to vary in a manner to reduce the frequency difference between the cable tuner input signals and the signals at the output of the receive block [3].

Once the signals have gone through the cable tuner receive block, they are ready to be digitally processed according to the application.

This report focuses on the design and operation of the first-stage differential LNA of the cable tuner.

4.0 DESIGN METHODOLOGY

The design of the LNA circuit was a step-by-step process that was divided into the following tasks:

4.1 Overall Cable Tuner and First-Stage LNA Specifications

4.2 Selection of Circuit Technology

4.3 Circuit Topology

4.4 Making the LNA Circuit Differential

4.5 Sizing all Circuit Components and Impedance Matching

The rationale for this division of tasks was to organize the design process in a logical manner starting with the specifications and transistor technology, followed by the choice of circuit topology and finally, impedance matching and sizing the circuit components to meet the requirements.

4.1 Overall Cable Tuner and LNA Specifications

In order to begin the LNA design, Professor Rogers supplied the specifications for the overall cable tuner and the first-stage LNA and mixer. These specifications are listed in Table 4.1.1. Given the first-stage Noise Figure, the number and power level of input tones, and the Composite Triple-Order Beat, the theoretical Noise Figure, Input and Output Third-Order Intercept Points (IIP3 and OIP3) of the LNA were calculated. The complete calculations are provided in Appendix A of the report and the results are summarized in Table 4.1.2.

Table 4.1.1 Specifications for Overall Cable Tuner

Supply Voltages	3.3 V
Number of input channels	135 Tones
CTB (Composite Triple-Order Beat)	≤ 50 dBc
NF (Noise Figure)	≤ 9 dB

Table 4.1.2 Specifications for First-Stage LNA and Mixer

	LNA	Mixer
Voltage Gain	12 dB	4 dB
Total Current	20 mA	25 mA
Input Impedance (Z_{in})	75 Ω	
Noise Figure (NF)	≤ 10 dB*	
Input/Output Third-Order Intercept Point (IIP3/OIP3)	13.4 dBm* 25.4 dBm*	
Image Rejection (IR)	> 10 dB	

*Refer to Appendix A for the calculations of NF, IIP3 and OIP3

4.2 Selection of Circuit Technology

Once the specifications for the LNA were obtained, the next important choice that had to be made was the selection of appropriate transistor technology. For this project, 0.18 μm CMOS technology was chosen, which meant that all transistors used in the LNA circuit have a minimum length of 0.18 μm . This technology was chosen in favour of 0.35 μm transistors for its improved transition frequency, f_T due to shorter length parameter. In addition, NMOS devices were used instead of PMOS transistors because their higher transconductance also allows for an improved f_T .

With this technology, one important issue that had to be taken into consideration was the Body Effect. The Body Effect occurs when the bulk and source of the transistor are not at the same potential, resulting in a bulk-to-source voltage, V_{bs} [5]. The presence of V_{bs} increases V_T , the transistor threshold voltage according to the formula:

$$(4.1.1) \quad V_T = V_{T0} + \gamma \left(\sqrt{2\phi_f + V_{bs}} - \sqrt{2\phi_f} \right) \quad [6]$$

where γ = Body Effect parameter
 ϕ_f = Fermi Energy level
 V_{T0} = Zero bias threshold voltage

To minimize the Body Effect, the bulk and source of the transistors must be connected. For this reason, the bulks of all transistors were connected to the point of lowest potential in the circuit: on-chip ground. In doing so, the Body Effect was reduced in the transistors whose sources are also connected to ground. However, for certain transistors in the circuit whose sources are not grounded, the Body Effect cannot be neglected.

With the 0.18 μm NMOS technology selected, the next step was to develop an appropriate circuit topology to meet the design requirements.

4.3 Circuit Topology of the LNA

The circuit topology used for the LNA is directly related to its role as the first block of the cable tuner. The main functions of the LNA are to amplify and maintain the linearity of the cable tuner input signals and to minimize the amount of noise added to the system over a broad bandwidth. To satisfy the gain, input impedance, noise, and linearity requirements, the LNA was built using a Common-Source amplifier with a feedback loop, arranged in a cascode configuration with a Common-Gate amplifier. A current mirror biases the Common-Source/Common-Gate amplifier and an output buffer stage is included as well for added design benefits [1].

4.3.1 The Common-Source Amplifier

The Common-Source (CS) amplifier acts as the driver of the LNA. This topology, seen in Figure 4.3 (a), was chosen because it provides a high voltage gain, which is an important requirement of the design. In addition, the CS amplifier provides good linearity, which is due to the degeneration resistor, R_S , connected at its source [1].

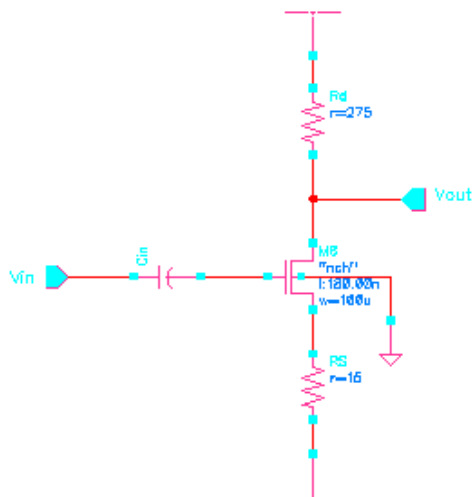


Figure 4.3(a) Common-Source Amplifier

While the CS configuration does satisfy the high gain requirement, it also has several drawbacks, including relatively high output impedance. However, the biggest drawback of the CS amplifier is its limited high-frequency response, which is due to the presence of C_{gd} , an internal capacitance that is connected between the gate and drain [2]. This can be seen in the small-signal circuit model of Figure 4.2 (b).

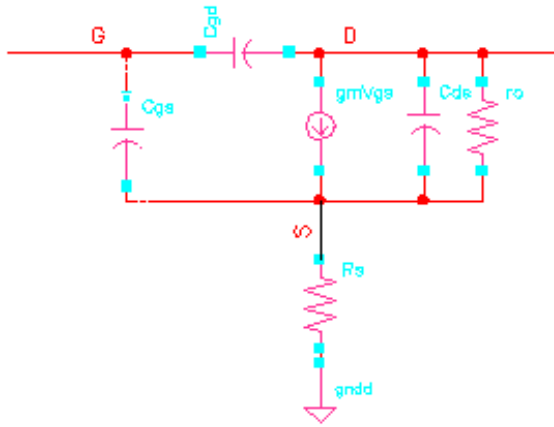


Figure 4.3(b) Small-Signal CS Circuit

Using Miller's Theorem, the capacitance C_{gd} may be split into two capacitances given by

$C_{gd} \cdot (1 - A_v)$ at the input and $C_{gd} \cdot \left(1 - \frac{1}{A_v}\right)$ at the output, where A_v is the voltage gain of the amplifier [7].

The new Miller equivalent circuit is given in Figure 4.3 (c). Since the voltage gain is negative and very large, the equivalent capacitance between the gate and source is also very large, resulting in a low high-frequency pole given by:

$$p_1 = \frac{1}{R_{in} \cdot C_{gs} \parallel [C_{gd}(1 - A_v)]} \approx \frac{1}{R_{in} \cdot (C_{gs} + C_{gd} A_v)}$$

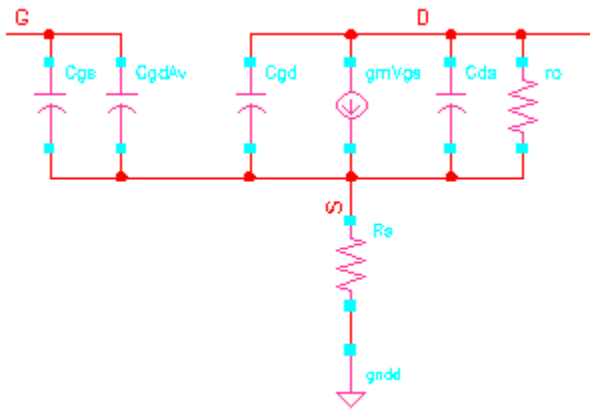


Figure 4.3(c) Miller Equivalent CS Circuit

It was necessary to improve the high-frequency performance of the LNA because it must be able to handle signals at frequencies as high as 850 MHz. To reduce the effects of these characteristics on the performance of the LNA, the CS design was modified.

4.3.2 The Cascode Amplifier

In order to improve the high-frequency behaviour of the LNA, the cascode configuration was employed, where the CS amplifier is connected in cascade with a Common-Gate (CG) amplifier, as seen in Figure 4.3 (d).

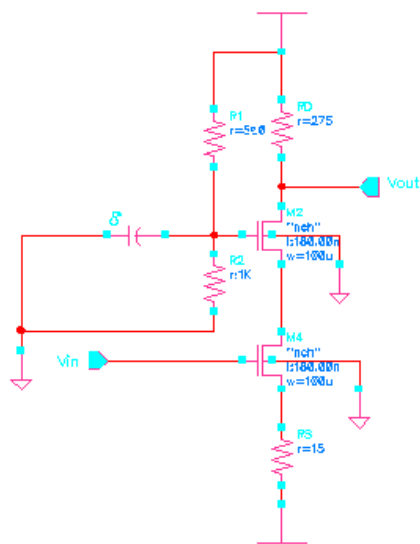


Figure 4.3(d) Cascode CS-CG Amplifier

By itself, the CG amplifier has a much wider bandwidth than the CS amplifier because it does not suffer from the same Miller effect. In the small-signal equivalent circuit of Figure 4.3 (e), it can be seen that the gate of the CG amplifier is shorted to ground at AC, which means that one side of its internal capacitance, C_{gd} , is grounded as well [2].

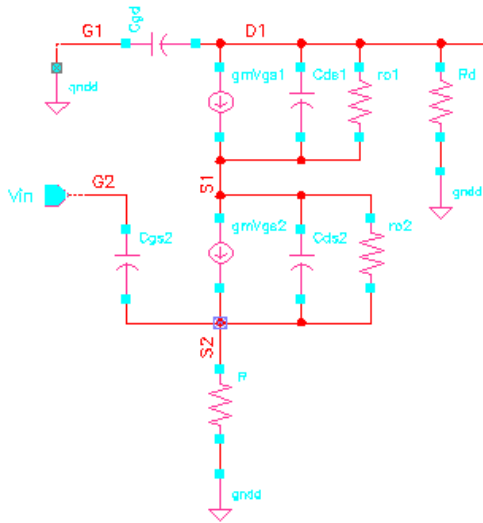


Figure 4.3(e) Small-Signal Cascode Circuit

When the two amplifiers are arranged in cascade, the role of the CG amplifier is to decrease the Miller Effect on the CS amplifier by decreasing its voltage gain. The voltage gain of the CS amplifier is given by: $A_v \approx g_m r_{out} \parallel R_L$ and when the CG amplifier is added, the output resistance

seen by the CS amplifier is approximately $\frac{1}{g_m}$. With a decrease in voltage gain, the high-

frequency performance of the LNA is improved because the equivalent Miller capacitance at the input, $C_{gd} \cdot (1 - A_v)$, is reduced. Therefore, the input high-frequency pole is higher than the pole that results from the CS amplifier alone.

While an improvement in high-frequency performance is the primary advantage of the cascode design, this configuration may also have a negative effect on the linearity of the circuit due to the stacking of the two transistors [1].

4.3.3 DC Biasing Circuitry

Once the CS-CG cascode configuration was established, it became necessary to find a method of properly biasing the cascode transistors. The current mirror of Figure 4.3 (f) is one method of generating a stable reference current that can be used to produce proportional DC currents for biasing other transistors in the circuit [2]. In this case, the current mirror was built using two nfet devices, one being the transistor of the driving CS amplifier. The biasing transistor, like the CG transistor, has a degeneration resistor connected at its source. The biasing transistor is fed with a reference current, which is fixed using a DC source and a reference resistor, and the output current is taken at the drain of the CS amplifier. Since the two transistors are connected in parallel, they have the same gate-source voltage, V_{gs} . As long as both transistors are operating in the saturation region, where $V_{gs} > V_t$ and $V_{ds} > V_{gs} - V_t$ for the CS transistor, the output drain current of the CS amplifier is a function of the reference current, as well as the width and length of both transistors [6]. By adjusting the width parameter of each transistor, the mirror was scaled and the drain current of the CS amplifier was fixed.

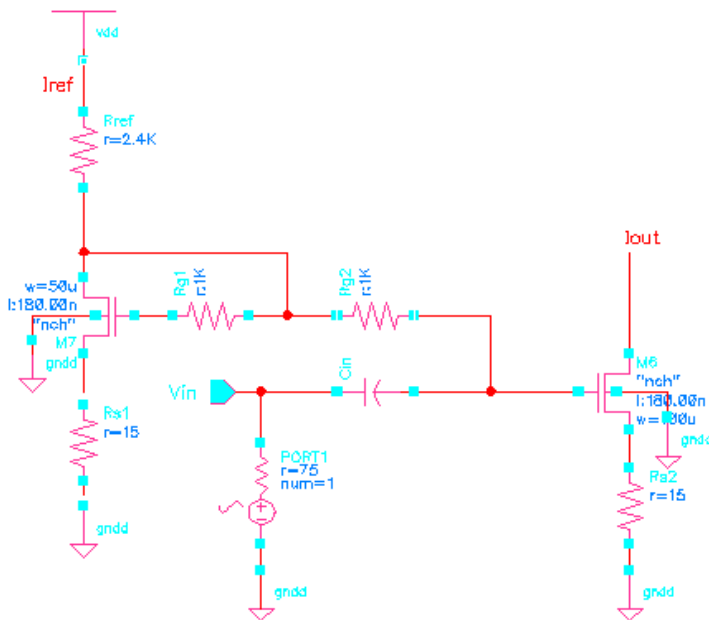


Figure 4.3(f) Input Current Mirror

The DC biasing of the CG amplifier was accomplished using a voltage divider between two resistors connected at its gate, as seen in the cascode configuration of Figure 4.3 (d). These resistors allow the CG amplifier to operate in the saturation region and to be properly biased at DC. To ensure that these biasing resistors did not affect the AC operation of LNA, a coupling capacitor was included to act like an AC short-circuit and ground the gate.

4.3.4 The Feedback Loop

When the DC conditions had been properly met using the cascode amplifier biased by a current mirror and a pair of biasing resistors, a further addition was made to the circuit configuration. A feedback loop from the drain of the CS amplifier back to the input gate was added. The CS amplifier with feedback loop can be seen in Figure 4.3 (g).

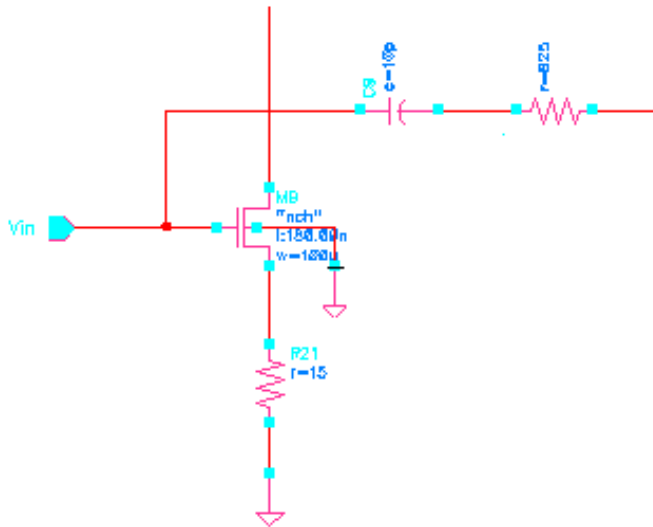


Figure 4.3(g) CS Amplifier with Feedback loop

The feedback loop consists of a resistor and a capacitor. The capacitor, C_f , allows the gate and drain to be biased independently by acting as an open-circuit at DC, while the resistor, R_f , provides the most significant advantage of using the feedback loop. The inclusion of this component allows the LNA to be matched over a broad bandwidth because its input impedance

is largely dependent on R_f [1]. Other additional benefits of matching the source impedance to the input impedance are maximum output power and improvement to the overall noise performance of the LNA. [2].

As with the cascode configuration, there are tradeoffs that go along with using a feedback loop. In this case, the overall gain of the LNA is reduced due to the presence of R_f in the circuit [1].

4.3.5 The Output Buffer Stage

The final modification that was made to the LNA design was the inclusion of an output buffer stage, seen in Figure 4.3 (h), which acts as the driver to the first-stage mixer. The main purpose of the output buffer stage is to provide autonomy between the cable tuner circuit blocks because it has both high input impedance and low output impedance [1]. The output buffer is a good lead-in to the mixer because it ensures that the LNA gain will not be affected by any changes to the input impedance of the mixer. Furthermore, the buffer also reduces the effect of R_f on the LNA voltage gain [1].

In order to establish a steady-state current to the buffer stage, another current mirror was added to the circuit topology. The output current of the mirror configuration was fed into the buffer stage.

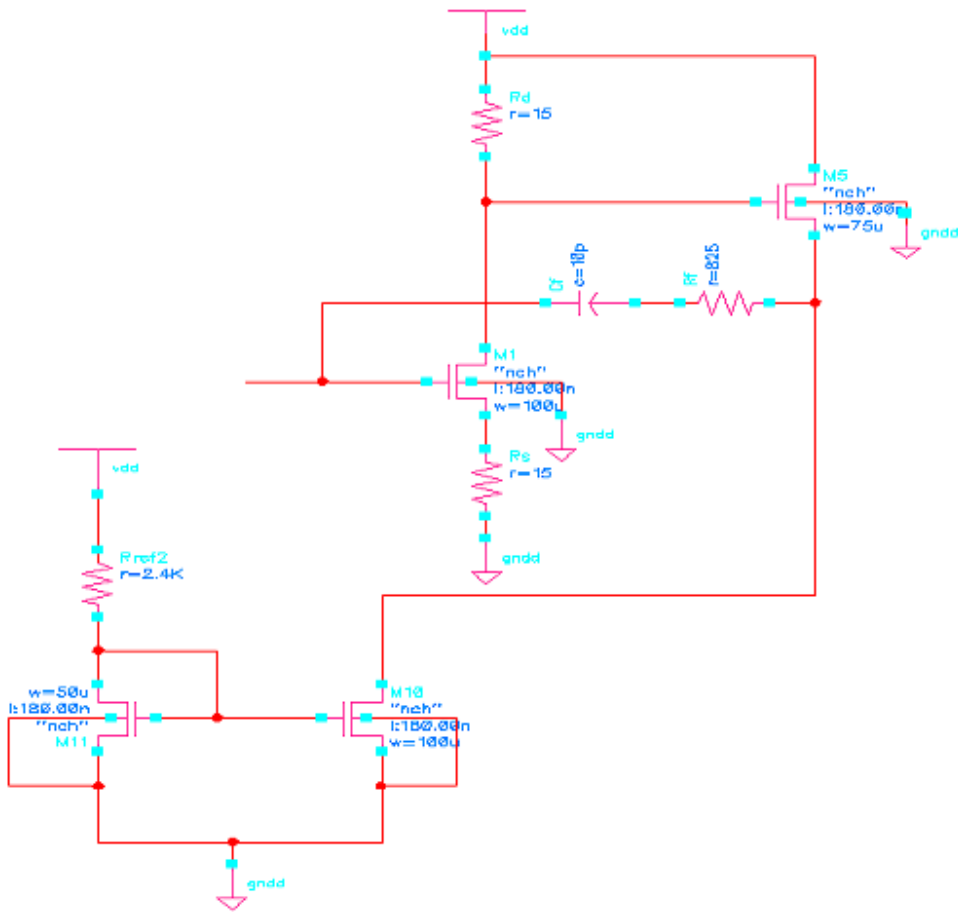


Figure 4.3(h) CS Amplifier with Output Buffer Stage

Once the output buffer stage was added to the design, the circuit topology of the LNA was complete. The full circuit, consisting of a CS amplifier, arranged in cascode with a CG amplifier and extended to include a feedback loop and an output buffer stage, is given in Figure 4.3 (i). The LNA circuit was designed in this manner to achieve the desired gain, input impedance, noise figure and linearity requirements.

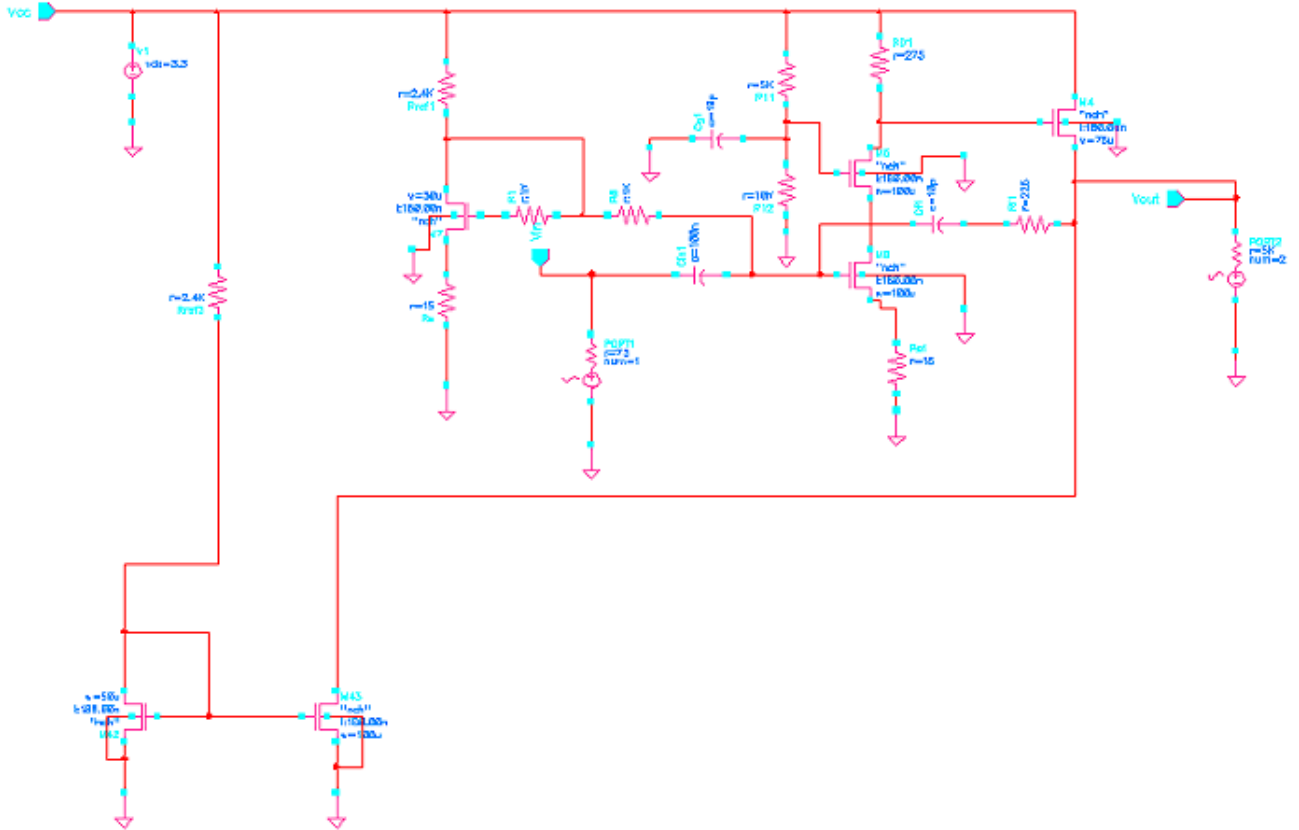


Figure 4.3(i) LNA Differential Half-Circuit

4.4 Making the LNA Differential

Once the LNA circuit topology was complete, it became necessary to make the circuit differential. Differential circuits are an important part of integrated circuit design because they offer several important advantages over single-ended circuits [2]. The first important advantage the differential LNA offers is a stable reference point. With any type of circuit, the measured values are always taken with respect to a reference. In the case of a non-differential LNA in the cable tuner, this reference would be on-chip ground. However, the on-chip ground may not be very reliable due to the presence of parasitic resistance and capacitance, leading to unpredictable results. By contrast, with a differential LNA, the measured results of one half-circuit are always taken with respect to the other half-circuit. This minimizes the chances of getting unexpected results [1].

Another significant and relevant benefit of using a differential circuit is noise reduction. Provided the noise source at the input of the amplifier is distributed equally between the incoming signal lines such that they see the same input noise, the noise will not be amplified by the same gain factor as the input signals [6].

In order to make the LNA circuit of Figure 4.3 (i) differential, another half-circuit was built, where each transistor and circuit component has a complimentary transistor or component. The positive input voltage is measured at the gate of one of the half-circuit CS amplifiers, while the negative input voltage is measured at the gate of the other half-circuit. The overall output of the LNA is measured between the sources of each half-circuit. In this case, it is now the difference between the two input signals that is being amplified [5]. The complete differential LNA can be seen in Figure 4.4.

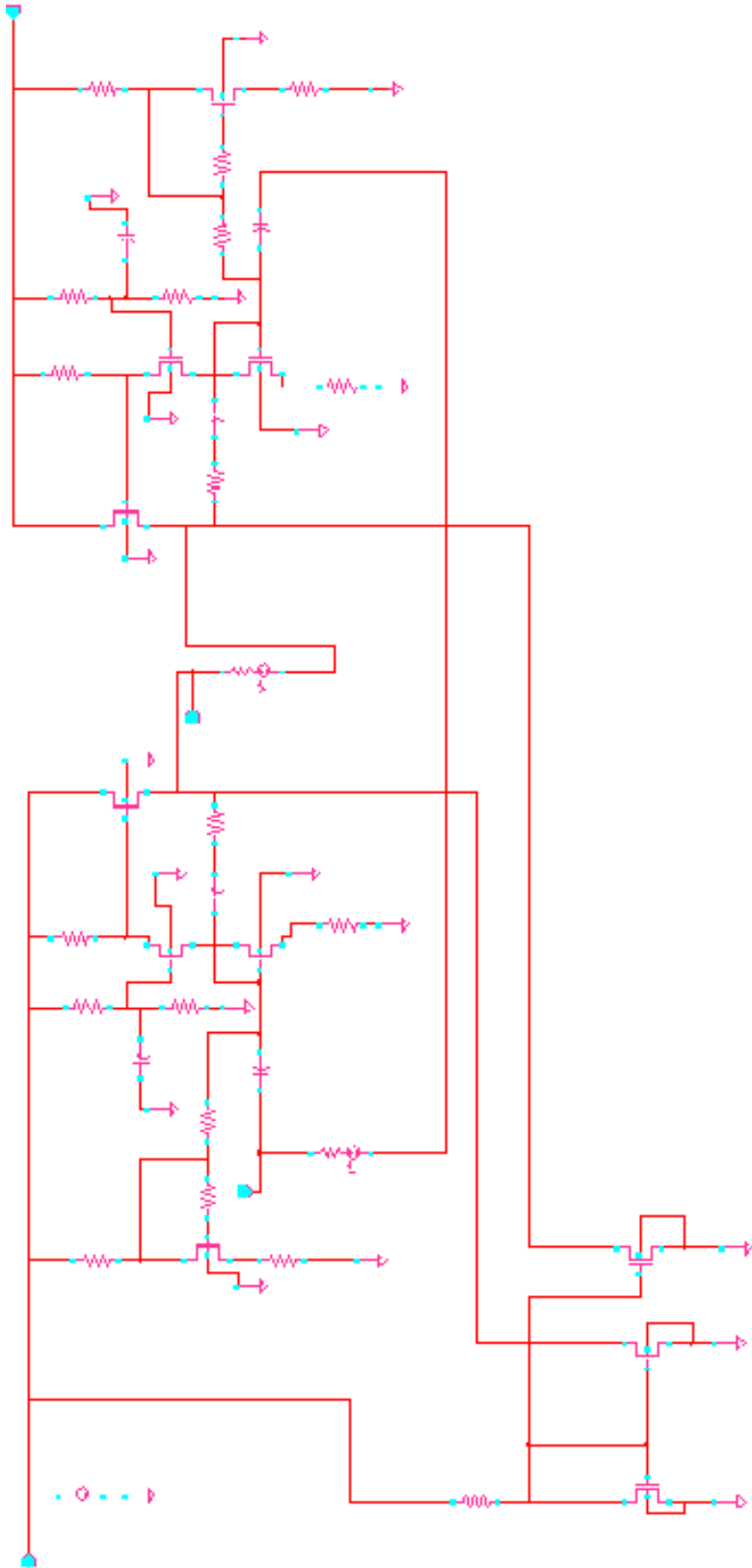


Figure 4.4 Differential LNA

4.5 Sizing all Components and Impedance Matching

With the LNA now set up as a differential circuit, the sizing of all components was the last step to be done before starting the simulation process. It is important to note that all component values given to one half-circuit also apply to the other half-circuit since they are identical.

The total current available for each half-circuit was 10 mA, which was divided between the output buffer stage and the CS amplifier driver stage. To begin, 3 mA of current was allocated to the output buffer stage. As a result, there was 7 mA of current available for the driver stage.

To begin the sizing process, the DC operation of the LNA was examined. It was found that in order to meet the gain and input impedance specifications, it was necessary to increase the transconductance of the driver stage transistors. The transconductance is the constant that relates I_{ds} and V_{gs} and is given by the following formula:

$$(4.5.1) \quad g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \mu_n C_{ox} (V_{gs} - V_t) \quad [6]$$

where μ_n = electron mobility

C_{ox} = capacitance per unit area of the gate-to-channel capacitor

This equation applies to transistors operating in the saturation region and indicates that the value of g_m depends on the $\frac{W}{L}$ ratio of the transistor. To increase the g_m of any transistor in the circuit, it was necessary to increase its width or decrease its length. For this design, the lengths of all transistors were set to 0.18 μm in order to keep the sizes of all transistors to a minimum

and reduce the layout area. However, the widths of the driver CS-CG transistors were adjusted to 200 μm each.

Once the transconductance of the driver transistors was improved, the current mirror for the driver stage was set up. With the biasing and CS transistors operating in saturation such that $V_{gs1} = V_{gs2} > V_t$ and $V_{ds2} > V_{gs2} - V_t$, the current mirror reference current, I_{ref} was established.

The formula for I_{ref} is given by:

$$(4.5.2) \quad I_{ref} = \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} (V_{gs} - V_t)^2 \quad [2]$$

and was chosen to be 1 mA. To get a reference current of 1 mA, a resistor was placed at the drain of the biasing transistor, whose value was determined to be:

$$(4.5.3) \quad R_{ref} = \frac{(V_{dd} - V_{gs})}{I_{ref}} = \frac{(V_{dd} - (V_t + V_{safety}))}{I_{ref}} = 2.4k\Omega \quad [6]$$

In this case, the threshold voltage for the transistor model was found in the model files to be 0.3628 V and the safety voltage was selected to be 200 mV [6].

Since the drain current of the CS amplifier is a function of I_{ref} and the transistor width and length parameters, its value was set to 4 mA by scaling the current mirror according to the formula:

$$(4.5.4) \quad I_{out} = I_{ref} \frac{\left(\frac{W_2}{L_2}\right)}{\left(\frac{W_1}{L_1}\right)} = 1mA \cdot \frac{200\mu m / 0.18\mu m}{50\mu m / 0.18\mu m} = 4mA \quad [2]$$

The current mirror was scaled so that the width of the biasing transistor was set to 50 μm , resulting in a current mirror ratio of 1:4 and a drain current in the driver transistor of 4 mA.

A 1 k Ω resistor was also placed at the gates of the current mirror transistors to provide RF isolation between the current mirror and the driver stage of the LNA [1].

A similar approach was used to size the current mirror of the output buffer stage. In this case, the current mirror was scaled to have a ratio of 1:2. By scaling the mirror, the total current consumed by the circuit was reduced. The lengths of the transistors remained the same, but the biasing and output buffer transistor widths were set to 50 and 100 μm respectively. Since the current of this stage was set to 3 mA, the reference current had to be fixed at 1.5 mA according to equation (4.5.4). Equation (4.5.3) was then used to calculate the value of the reference resistor to be 2.4 k Ω .

The DC biasing of the CG amplifier was also done, this time using a voltage divider between two biasing resistors. The gate voltage of the CG amplifier was set to 2.2 V according to the formula:

$$(4.5.5) \quad V_g = V_{dd} \cdot \frac{R_2}{R_1 + R_2} = 2.2V$$

R2 was chosen to be 10 k Ω and from Equation (4.5.5), R1 was calculated to be 5 k Ω . To ensure that the biasing resistors did not interfere with AC operation of the LNA, the gate was short-circuited to ground using a large capacitor, $C_g = 10$ pF. Another coupling capacitor, C_{in} , was set to 10 pF and placed at the gate of the CS amplifier to act as an open-circuit during DC operation.

The next resistors that required sizing were the drain resistor, R_d , and the degeneration resistor, R_s . These values were assigned according to the equation for voltage gain of the differential circuit. The voltage gain of the differential LNA can be approximated by:

$$(4.5.6) \quad A_v = \frac{R_d}{R_s + \frac{1}{g_m}} \quad [2]$$

It follows that the value of R_d must be set high enough and R_s set low enough to satisfy the gain requirement. The values of R_d and R_s were set to 275 Ω and 15 Ω respectively. It was found that setting R_s to 15 Ω allowed for the gain, noise, and linearity specifications to be met simultaneously. By making this resistor larger, the linearity of the LNA did improve, but to the detriment of the gain and noise results. Similarly, when the resistor value was reduced, the gain and noise in the circuit improved, but the linearity decreased. For this reason, the degeneration resistor of the driver transistor and the biasing transistor were set to 15 Ω each.

The last components to be sized were R_f and C_f of the feedback loop. This is because R_f plays a large part in determining the input impedance of the LNA. At this point, it became necessary to match the input impedance of the LNA to the source impedance of 75 Ω . Because the half-circuits are identical, each half-circuit needed to be matched to 37.5 Ω , making the entire circuit matched to 75 Ω . The input impedance of the CS amplifier with a feedback loop and an output buffer is approximated by:

$$(4.5.7) \quad Z_{in} = \frac{R_f}{g_m \cdot R_d} \quad [2]$$

From this formula, the feedback resistor was set to 225 Ω . The feedback capacitor, C_f , was given a value of 10 pF, which is high enough to ensure that at DC, it would behave as an open-circuit so the gate and drain could be biased independently. The drain resistor, R_d , was set to 275 Ω , which allowed for both the gain and input impedance requirements to be satisfied.

The output buffer transistor was the last transistor to be sized. As stated previously, the output buffer acts as a driver to the first-stage mixer and therefore, it must have low output impedance. The output impedance of the buffer stage can be approximated as:

$$(4.5.8) \quad Z_{out} = \frac{1}{g_m} \quad [2]$$

Since the output impedance and transconductance of the buffer are inversely proportional, it was necessary to increase g_m to reduce Z_{out} . The width of the output buffer transistor was increased to 75 μm such that g_m was increased according to equation (4.5.1) and Z_{out} was decreased.

At this point, the DC operation of the LNA was established and all transistors and circuit components were sized. The LNA was built using Cadence software and ready to be tested to ensure that it met specifications.

5.0 SIMULATION RESULTS

The different types of analysis that were performed on the LNA are DC, AC, Noise, scattering-parameter (s-parameter), and periodic steady-state (PSS) analysis. These analyses were done in order to determine the total current, voltage gain, input impedance, noise figure, and input third-order intercept point of the LNA. The simulation results, along with the specifications from Section 4.1, are summarized in Table 5.0, and discussed in greater detail in the following sections.

Table 5.0 Comparison of Theoretical and Simulation Results

	Theoretical	Simulation
Total Current	20 mA	20.54 mA
Voltage Gain	12 dB	12.6-14.0 dB
Input Impedance	75 Ω	79 Ω
Noise Figure	5.34 dB	5.5-6.0 dB
Input Third-Order Intercept Point (IIP3)	13.4 dBm	7.20 dBm (low) 9.21 dBm (mid) 8.69 dBm (top)

5.1 Total Current

When a DC analysis was performed, the total amount of current being consumed by the LNA was measured to be 20.54 mA. The total current available for the LNA according to the specifications of Table 5.0 is 20 mA, which means that the current consumption of the circuit agrees with the specification.

5.2 Voltage Gain

The voltage gain was measured from the AC analysis as the difference in decibels between the output voltage and input voltage. The plot of the voltage gain in Figure 5.2 shows the voltage gain of the LNA throughout the frequency band of 50 to 850 MHz. The voltage gain is at its maximum at the start of the frequency band, 50 MHz, and drops to a minimum at the end of the band. At the top end of the spectrum, the voltage gain reaches 14.0 dB and at the low end, the gain falls to 12.6 dB. According to the specifications given in Table 5.0, the required voltage gain for the LNA is 12 dB. These results are slightly above the requirement, but an overall LNA gain of 14.0 dB is still low enough to ensure that when the input signals are fed from the LNA into the mixer, it will not be overloaded.

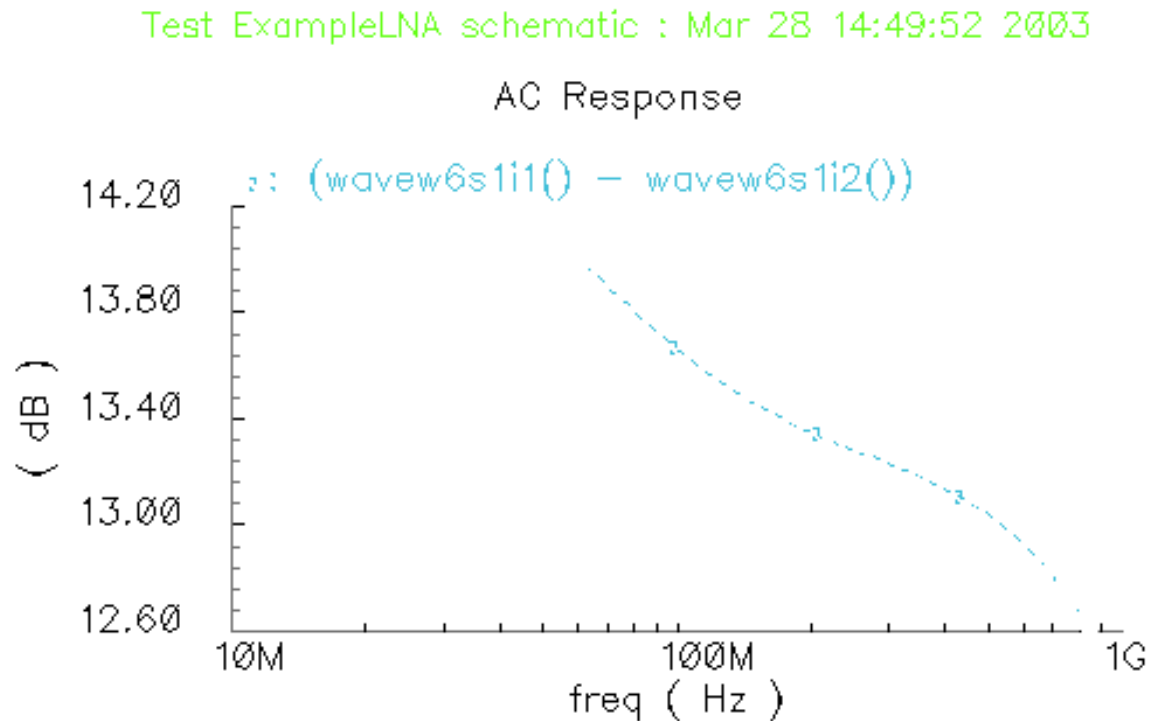


Figure 5.2 LNA Voltage Gain

5.3 Input Impedance

S-parameter analysis was used to measure the input impedance of the LNA. The input impedance, Z_{in} , is measured from the plot of S_{11} , where S_{11} represents the input reflection coefficient with the output properly terminated [4]. The input impedance, Z_{in} , of the LNA can be read from the S-parameter response Smith Chart of Figure 5.3. To interpret the Smith Chart results, it is important to define several values. Z_0 represents the reference impedance, which is the 75 Ω source resistance to which the circuit is being matched. The variable z represents the normalized impedance that can be read directly from the Smith Chart. Finally, Z represents the actual impedance of the circuit. The relationship between z , Z_0 and Z is given by:

$$(5.3.1) \quad z = \frac{Z}{Z_0} \quad [4]$$

From the Smith chart, it can be seen that the input impedance moves along a constant-resistance circle, $z = 1.052$. As the frequency increases, the capacitive reactance decreases and the impedance plot moves clockwise along this constant-resistance circle as the reactance becomes inductive [4]. Using the formula above, the input impedance Z_{in} of the LNA can be calculated as $Z_{in} = (1.052)(75) = 79 \Omega$. This result shows that the LNA is very closely matched to the 75 Ω source impedance over a bandwidth of 50 to 850 MHz.

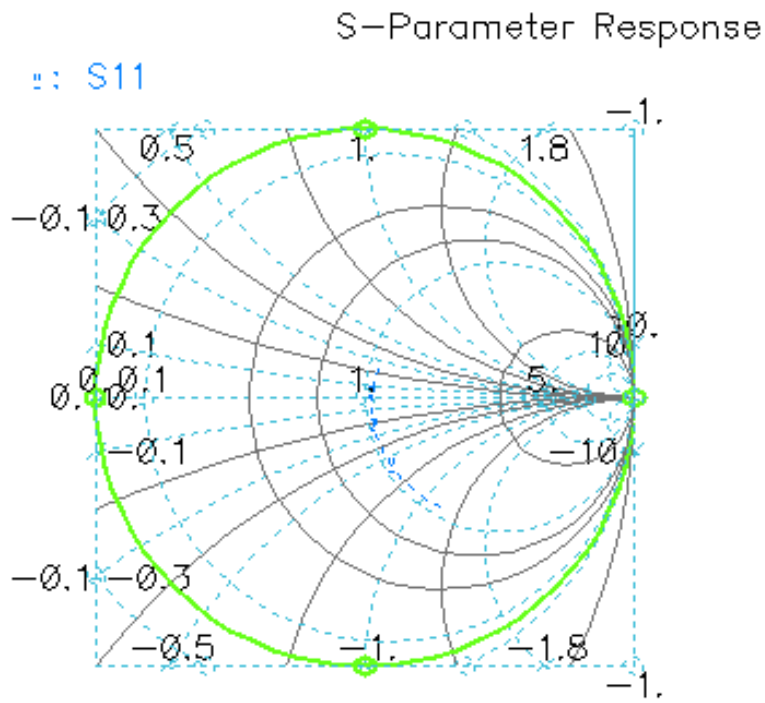


Figure 5.3 LNA Input Impedance

5.4 Noise Figure

S-parameter analysis was also used to generate the Noise Figure of the LNA. The Noise Figure plot is shown in Figure 5.4. According to this graph, at the top end of the spectrum, the noise figure reaches a maximum of 6.0 dB and reduces to a minimum value of 5.5 dB at the low end of the frequency band. The simulated result agrees very closely with the specified noise figure that was given in Table 5.0 to be 5.34 dB. In addition, the noise figure of the LNA remains fairly constant throughout the frequency band with only a 0.5 dB difference between the top and low ends of the spectrum.

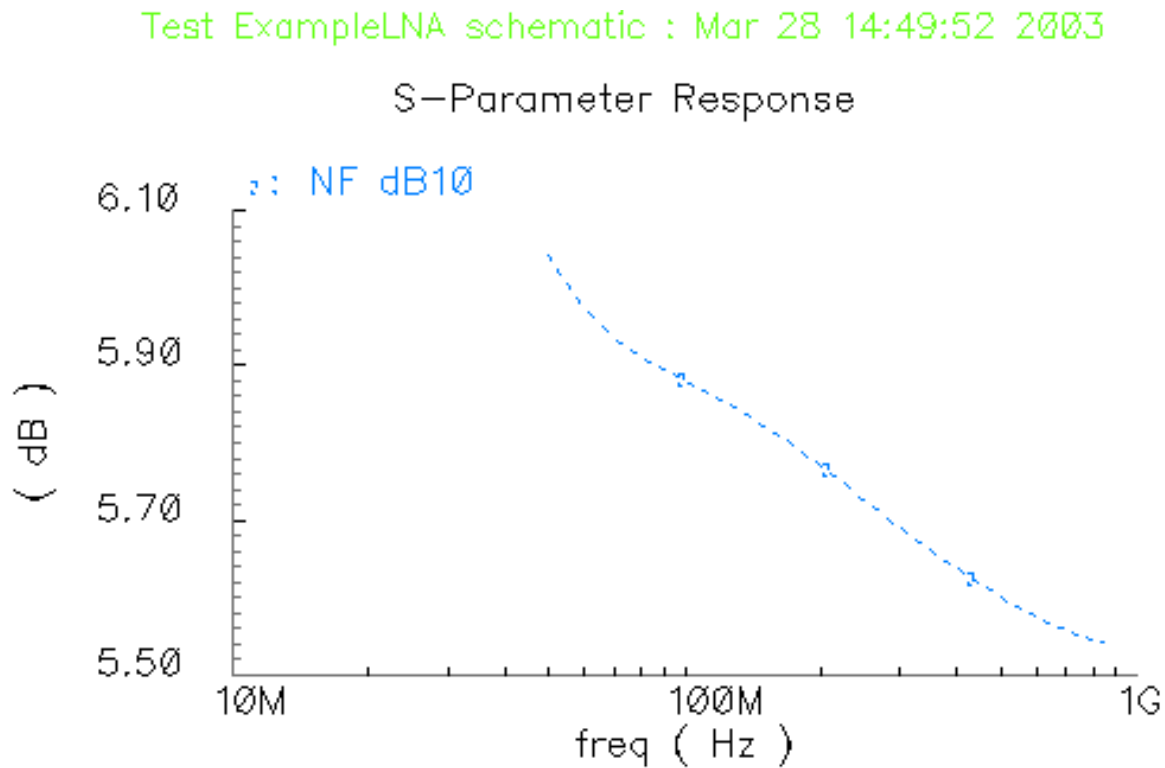


Figure 5.4 LNA Noise Figure

5.5 Linearity of the LNA

The final important analysis performed on the LNA was a PSS analysis to test the linearity of the circuit. This test was done by applying two tones at the input, RF_1 and RF_2 , which are separated by a small frequency of 5 MHz to extrapolate the input third-order intercept point (IIP3) [1]. The IP3 point is “a theoretical point where the amplitude of the intermodulation tones at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are equal to the amplitude of the fundamental tones at ω_1 and ω_2 ” [1]. It is important to be aware of the intermodulation signals as they are located very close to the fundamental, making them very difficult to filter out. The plots shown in Figures 5.5 (a), (b), and (c), show the IIP3 point of the LNA at the low end, middle, and top of the frequency band. As the two tones are moved across the band, the IIP3 goes from 7.2 dBm to 9.21 dBm, and drops to 8.69 dBm. These results indicate that the IIP3 point obtained from simulation varies slightly from the calculated value of 13.4 dBm, and is closest to the theoretical expectation in the middle of the frequency band.

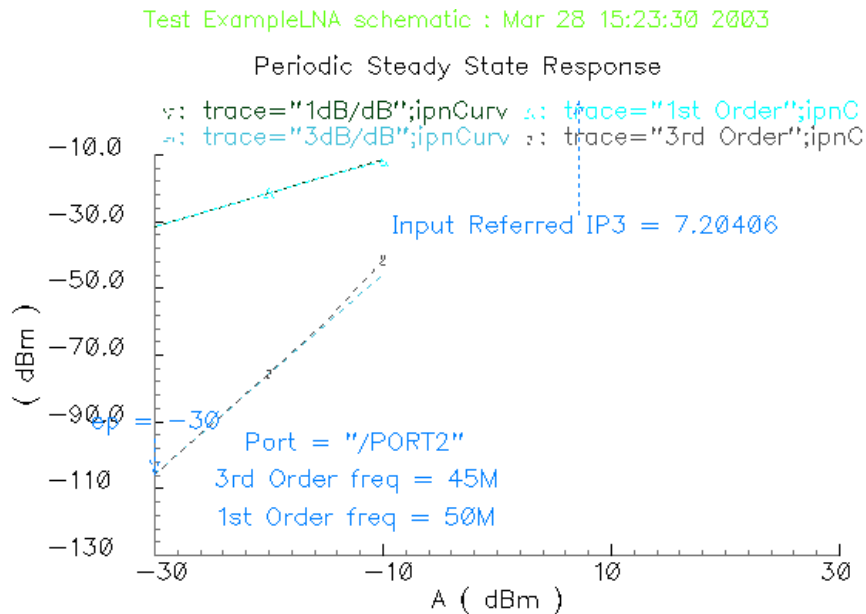


Figure 5.5(a) IIP3 at low end of frequency band

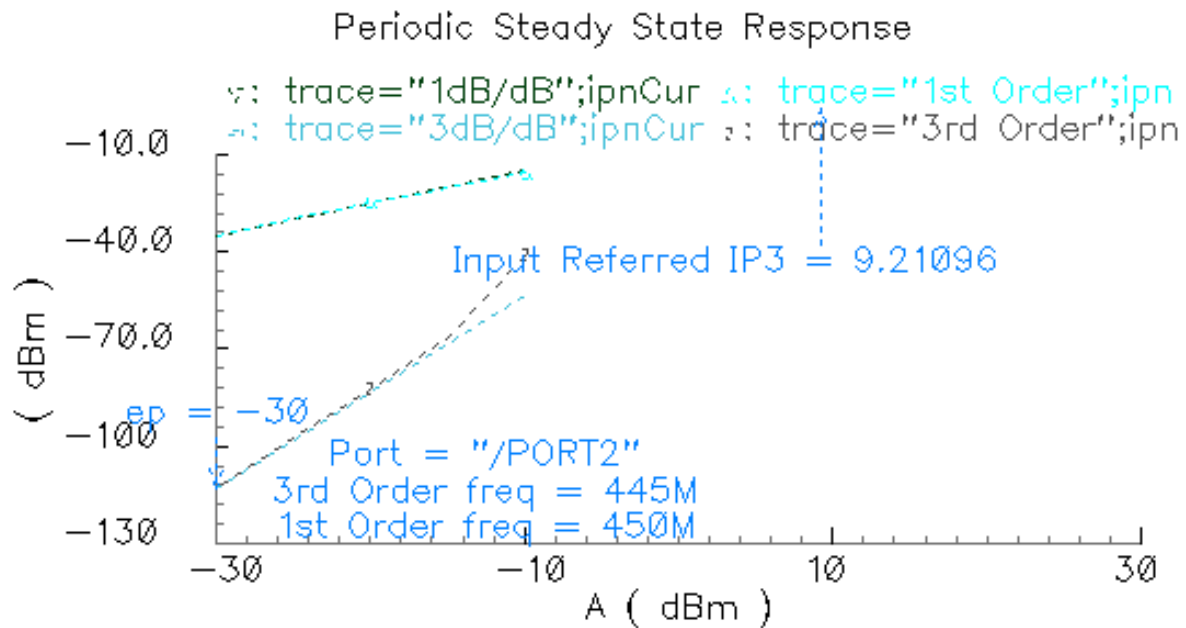


Figure 5.5(b) IIP3 at middle of frequency band

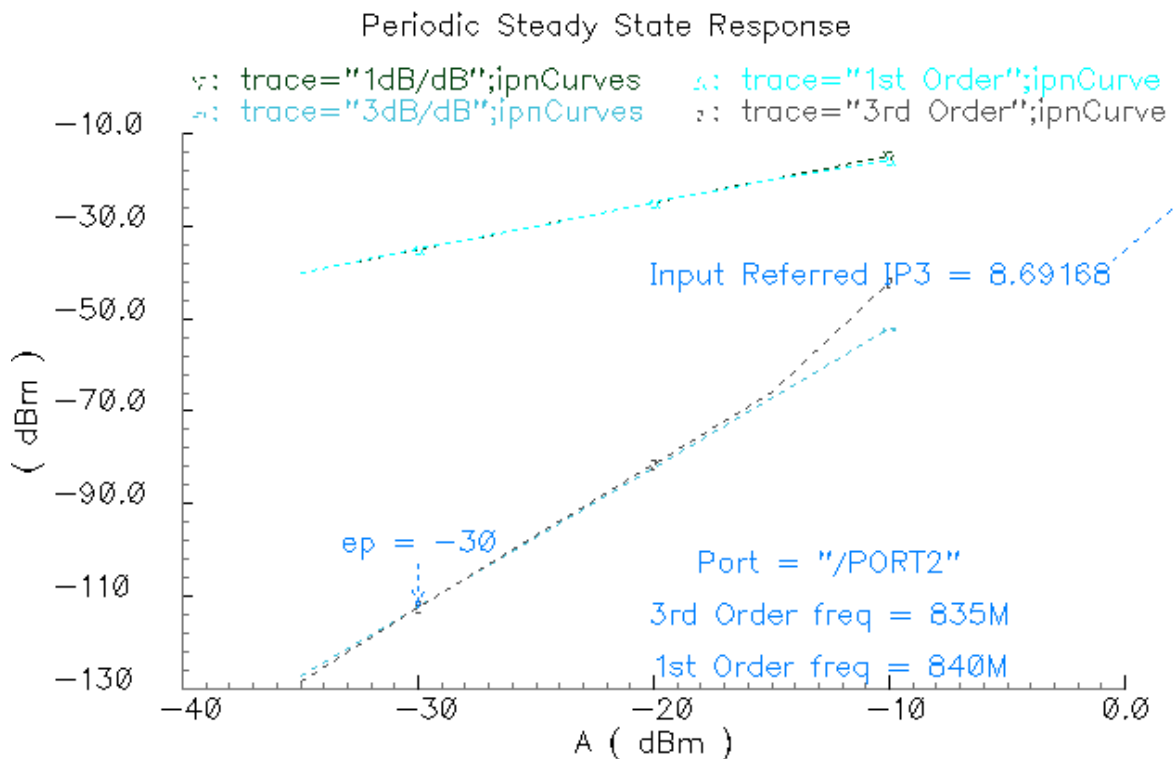


Figure 5.5(c) IIP3 at top of frequency band

6.0 LAYOUT

Once the design and simulation of the differential LNA were complete, the final phase of RFIC design that was explored was layout. Performing layout of the LNA was necessary for several key reasons. First, it was important to determine the amount of physical space the LNA would occupy since it will be placed on a chip of limited area. Because all of the cable tuner circuit blocks are located on-chip, the LNA must be built in such a way that it takes up as little space as possible. However, the most important reason for doing layout is because the physical design of the LNA largely determines its performance [7]. Since circuit devices are fabricated using various materials, “the physical structure determines the transconductances of the transistors, the parasitic capacitances and resistances, and obviously, the silicon area which is used to realize a certain function” [7]. All of these transistor parameters must be optimized in order to achieve high speed and minimum power dissipation.

6.1 Automatic versus Manual Layout

The process began with the physical layout of the LNA transistors. This was done using Virtuoso, which is the Cadence layout editor used to build and modify circuit components [7]. Along with Virtuoso, the Layer Selection Window (LSW) was used, which is the tool used to select different layers of material to build the circuit components [7]. For the physical layout of the LNA transistors, there were two possible methods for creating these components: manual and automatic layout. With manual layout, the user is required to build each transistor from scratch, using the LSW to select the appropriate materials for each layer. Once these layers are selected, the designer must fix their dimensions and configurations. Automatic Layout is the alternate choice for physical layout design. This type of layout uses a device level placer to read in a schematic and place all the transistors in the layout window [7].

For this project, the automatic layout process was initially selected because with a total of twelve transistors in the differential LNA circuit, using the manual layout technique to build each transistor would have been extremely time consuming. The device level placer was used to read in the differential LNA schematic of Figure 4.4 and place all the transistors. At this point, a drawback of automatic layout was discovered. While the automatic layout technique does save time by creating the transistors for the user, it does not build the transistors in a space-efficient manner. As described in Section 4.5, the device widths used in the LNA circuit topology were very large in order to meet the design specifications. The driver transistor widths were set to 200 μm and the output buffer was sized to 75 μm . The current mirror transistors were scaled to have widths of 50 μm and 100 μm each. Meanwhile, the lengths of all devices were set to a minimum value of 0.18 μm . When the transistors were generated automatically, they were created exactly according to these parameters, resulting in transistors with extremely large gate widths. Because the automatic tool did not optimize the design area it required for the transistors, it was discarded in favour of manual layout.

With manual layout, it was possible to create instances of transistors using the Virtuoso layout editor, but with this method, the width and length parameters could be adjusted. In order to avoid using transistors with gate widths of up to 200 μm , a technique known as gate splitting was used. By placing multiple devices in series, the gate width was split into smaller units known as fingers. The use of fingers allowed for smaller devices to be used, which optimized the total area occupied by the LNA circuit. With fingers, the correct gate width was still achieved, but with the essential benefit of a more compact design [7]. For the LNA design, the driver transistors were set up to have twenty fingers each, resulting in twenty smaller transistors with widths of 10 μm each. The output buffer was designed to have fifteen fingers, each having

a gate width of 5 μm . Lastly, the current mirror transistors were designed to have 10 fingers each, resulting in gates of 5 μm and 10 μm each.

With the transistors sized and placed, the next important step was to build the connections within and between the devices.

Because fingers were used to place multiple devices in series to achieve the total width of a single transistor, the resulting transistor needed to be connected properly. Having multiple fingers essentially broke the total transistor up into smaller sections. Therefore, each of these smaller sections needed to be tied together. The gates, drains, and sources of each finger were tied together using the same material from which it was created. An example of tying the nodes together can be seen in Figure 6.0 (a), which gives the output buffer current mirror built with multiple-finger transistors.

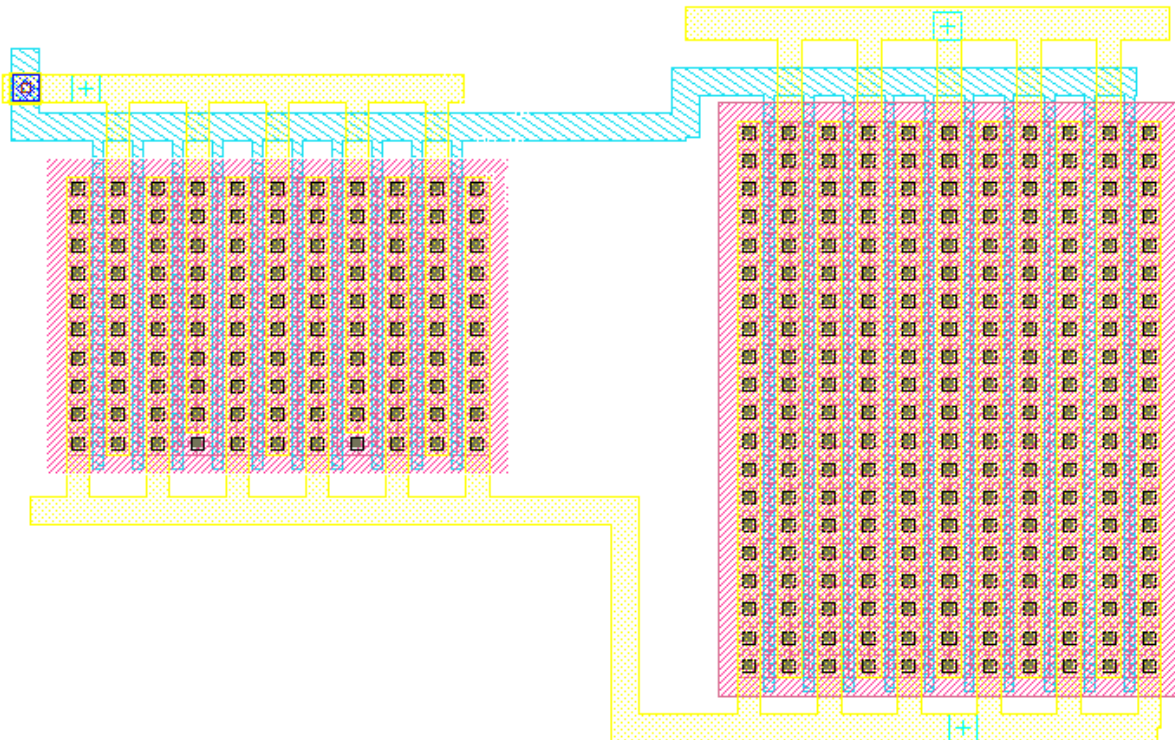


Figure 6.0(a) Layout of Transistors with Multiple Fingers

Establishing connections between devices was the next step in the LNA layout design. The cascode CS-CG amplifiers were connected by joining the source of the CG amplifier to the drain of the CS amplifier. Next, the driver stage transistors were connected to the output buffer transistors. This involved connecting the output buffer transistor and its current mirror bias to the drain of the cascode amplifier. The layout of the driver and output buffer stage transistors can be seen in Figure 6.0 (b).

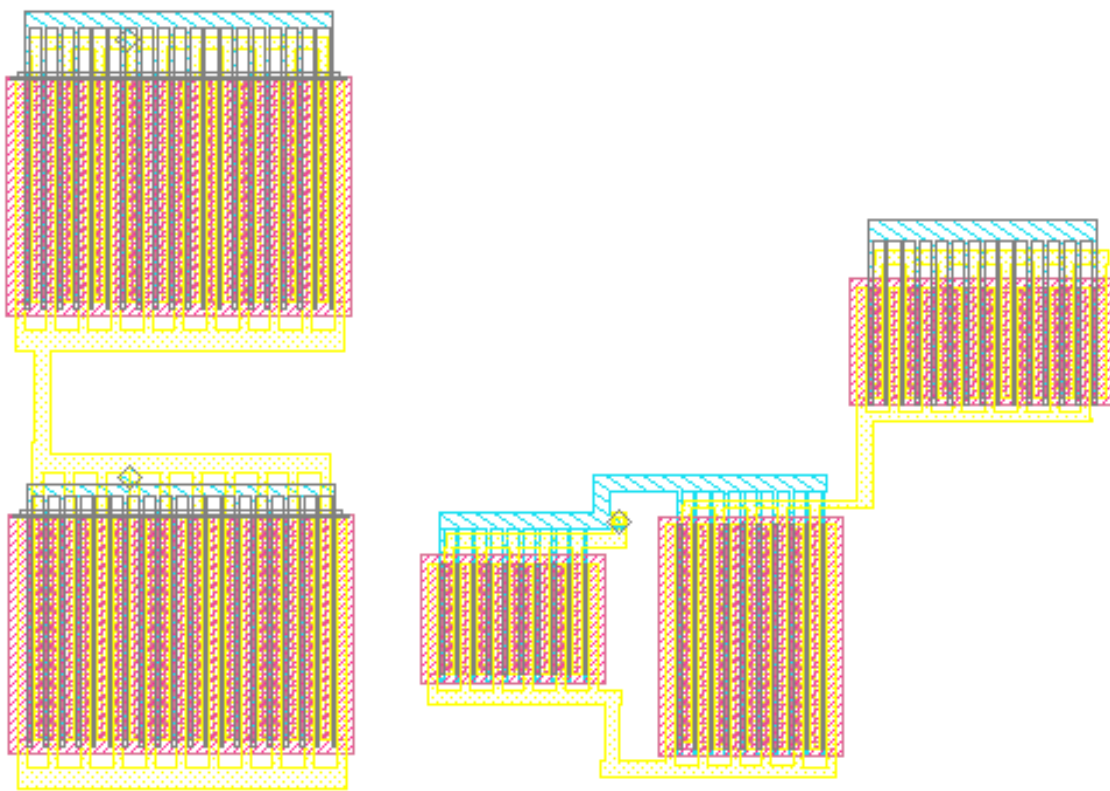
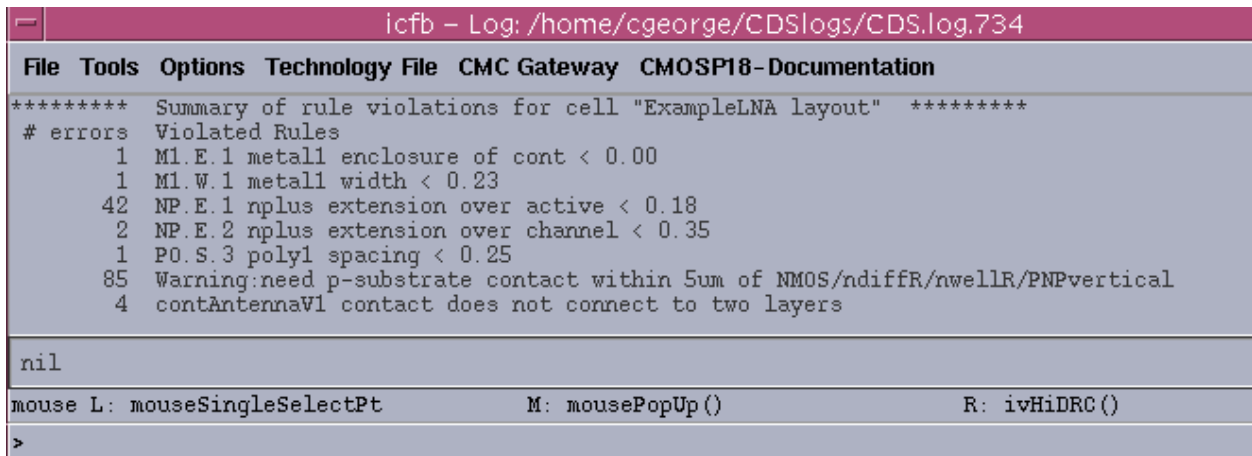


Figure 6.0(b) Layout of LNA Transistors

6.2 Design Rule Check (DRC)

Once the LNA transistors were laid out, the next task that was performed was a Design Rule Check (DRC). Any layout design “must conform to a complex set of design rules in order to ensure a lower probability of fabrication defects” [7]. These design rules specify the minimum dimensions for all transistor layers and contacts between layers.

When the Design Rule Checker was run on the layout of the LNA transistors, many design rule violations were detected. To illustrate the types of errors found by the DRC, a portion of the DRC results window is given in Figure 6.0 (c). At this stage of project, the LNA design work was completed.



```
icfb - Log: /home/cgeorge/CDSlogs/CDS.log.734
File Tools Options Technology File CMC Gateway CMOSP18-Documentation
***** Summary of rule violations for cell "ExampleLNA layout" *****
# errors Violated Rules
  1 M1.E.1 metall enclosure of cont < 0.00
  1 M1.W.1 metall width < 0.23
 42 NP.E.1 nplus extension over active < 0.18
  2 NP.E.2 nplus extension over channel < 0.35
  1 P0.S.3 poly1 spacing < 0.25
 85 Warning:need p-substrate contact within 5um of NMOS/ndiffR/nwellR/PNPvertical
  4 contAntennaV1 contact does not connect to two layers

nil
mouse L: mouseSingleSelectPt          M: mousePopUp()          R: ivHiDRC()
>
```

Figure 6.0(c) DRC Results for Transistor Layout

7.0 CONCLUSIONS

By taking into account the specifications for the first-stage LNA, the objectives established at the beginning of the project were largely achieved. The desired frequency range, voltage gain, and input impedance were achieved by selecting the appropriate circuit topology. By using low bias currents, the total current consumed by the LNA was reduced. Meanwhile, by ensuring that the noise due to resistors did not affect the AC operation of the circuit, the noise was minimized. Because the linearity of the LNA is slightly lower than the specification, it may be increased to improve the operation of the LNA.

The use of Cadence software facilitated the analysis of the results and allowed for comparisons between theoretical expectation and simulated results.

Although the LNA design was the primary focus of the project, a deeper understanding of the other cable tuner circuits was also developed. Through interaction and discussion with the project supervisor and team members, a better insight into design work and the application of engineering principles was gained.

8.0 RECOMMENDATIONS

Recommendations for this design project fall into two major categories: Improvement to simulation results through modifications to circuit design and development of layout, and the role of the LNA within the cable tuner and other applications.

8.1 Modifications to Circuit Design

In this project, the simulated results for total current, voltage gain, and input impedance meet the specifications stipulated at the start of the project. While the simulated noise figure and linearity results are close to the specified values, improvement to these values is still possible to meet the theoretical expectation.

In order to reduce the noise figure even further, it is necessary to examine the Noise Summary results of Figure 8.0 to determine the greatest contributors of noise to the circuit.

Device	Param	Noise Contribution	% Of Total
/PORT1	rn	4.18494e-18	24.52
/M6	fn	2.26586e-18	13.28
/M16	fn	2.19936e-18	12.89
/Rs2	rn	1.72334e-18	10.10
/Rs1	rn	1.70551e-18	9.99
/M6	id	1.32354e-18	7.76
/M16	id	1.2592e-18	7.38
/RD1	rn	4.44724e-19	2.61

Spot Noise Summary (in V²/Hz) at 1K Hz Sorted By Noise Contributors
Total Output Noise = 1.70641e-17
Total Input Referred Noise = 1.26727e-18

Figure 8.0 Noise Summary

From these results, it can be seen that the main sources of noise in the circuit are the degeneration resistors, R_s , and the driver CS transistor. The Noise Figure of the LNA is given by:

$$(8.1) \quad NF = 10\log(F), \text{ where } F = \text{NoiseFactor} = 1 + \frac{N_{added}}{N_{in} \cdot G} \quad [1]$$

and N_{added} = noise added to the system by the LNA

N_{in} = input noise

G = LNA gain

One method in which the noise due to this transistor may be reduced is by increasing the gain of the circuit. From equation (4.5.6), this means either decreasing the degeneration resistance, R_s , or increasing the drain resistance, R_d .

A higher third-order intercept point (IIP3) for the LNA may be obtained by increasing the degeneration resistor, R_s . However, it is important not to increase R_s too high because while this will improve the linearity of the LNA, it will also have an adverse effect on both the gain and noise of the circuit. To avoid the effects on gain and noise and to achieve an IIP3 of 13.4 dBm, the total current consumed by the LNA may be increased. This can be accomplished by increasing the size of the driver transistors.

8.2 Development of Layout

Layout is another important facet of the LNA design project that can be improved. Once the layout of all LNA components is complete and all errors have been successfully removed, there are a few additional steps that could be done to complete the layout process: Extraction, Layout Versus Schematic (LVS) Check, and Post-Layout Simulations.

Extraction involves the creation of a circuit description called a netlist. This netlist provides information regarding the transistors and their interconnections. It also identifies the device dimensions and the parasitic resistances and capacitances that affect its performance [7].

Once the LNA has been verified by the DRC and extracted, it can be compared to the original schematic of the LNA. The Layout versus Schematic Check (LVS) is a method of making sure that the layout has been implemented according to the original design schematic [7].

The final job that can be done as part of layout is to perform simulations of the extracted netlist so that the transistor-level performance of the LNA can be assessed. These post-layout simulations determine the speed and effect of resistive and capacitive parasitics on the LNA [7]. This final step enables the designer to determine if the post-layout simulation results agree with the original design specifications.

8.3 The Role of the LNA within the Cable Tuner

While it is essential that the LNA functions correctly on its own, it must eventually be integrated with the other circuit blocks to assess the performance of the cable tuner as a whole. Before the RF signals are passed to the second stage of the cable tuner, the unwanted image signals must be eliminated. Unlike the second-stage mixer, the first-stage mixer does not perform this task. For this reason, it is necessary to include an image-reject filter to the LNA circuit for this purpose. Once the first and second stages have been tested separately, the two stages can be connected and tested. Testing should be done at both the schematic and layout levels to ensure that the overall cable tuner specifications have been met.

8.4 Other Applications

For this project, the LNA was designed to meet the specifications of a cable tuner application. However, it is important to note that with variations to the circuit topology, the results can be optimized to meet different requirements and be used in other applications. For instance, the cascode CS-CG configuration may be replaced with another type of amplifier, depending on the main requirements of the design.

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