A 1.9GHz Gilbert Mixer in 0.18μm CMOS For a Cable Tuner

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The submission of this report is part of the partial fulfillment of the requirement for obtaining the Bachelor of Engineering Degree

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NOMENCLATURE

dB	Decibels
dBm	Decibels with respect to 1mW
DRC	Design Rule Check
DSB NF	Double-Sideband Noise Figure
F	Noise Factor
gm	Gate Transconductance of a MOSFET
IC	Integrated Circuit
IF	Intermediate Frequency
IM3	Third-Order Intermodulation Products
IP3	Third-Order Intercept Point
IIP3	Input-IP3
LNA	Lower Noise Amplifier
LO	Local Oscillator
NMOS	N-channel MOSFET
NF	Noise Figure
RF	Radio Frequency
R	Resistance
PSS	Periodic Steady State
SNR	Signal-to-Noise Ratio
SSB NF	Single-Sideband Noise Figure
VRF	Voltage Amplitude of RF signal
VLO	Voltage Amplitude of LO signal
VoIP	Voice Over IP

1.0 Project Introduction

The cable tuner is an RF broadband 50MHz - 850MHz signal receiver. Its purpose is to amplify the receiving signals, select the desire RF frequency within the range, and translate it to the intermediate frequency. There are many applications today that require the use of a cable tuner such as the cable internet modem and the television set. However, there can be many other uses for a cable tuner such as in VoIP, or any applications that require broadband channel selection. The major components of the cable tuner are the First Stage LNA and Mixer, Second LNA, Image Reject Mixer, and the PLL to control frequency selection.

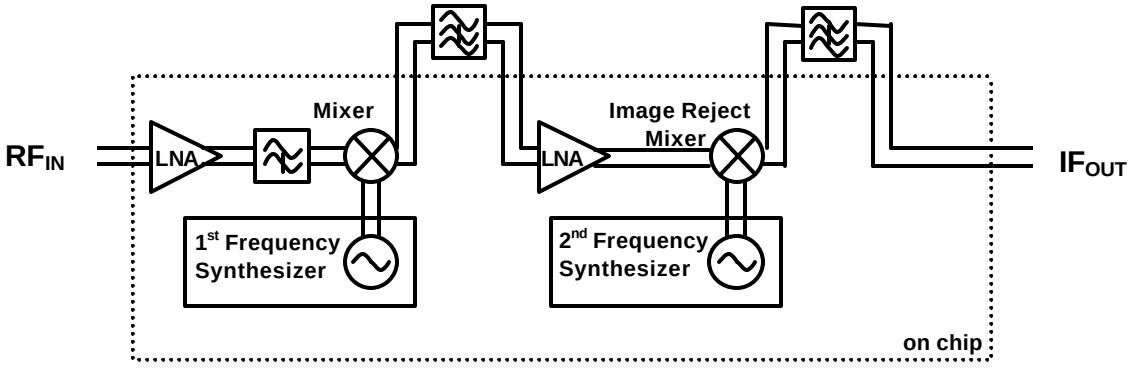


Figure 1 System Level Diagram of the Cable Tuner

For my 4th year project, I worked in a group under the supervision of Professor John Rogers to design the major components that make up a cable tuner. With the exception of the two filters shown on figure 1.0, all the components were designed to be integrated onto one chip. The task for each group member is shown in Table 1. My responsibility was for the design of the First Stage Upconverting Mixer. Our design was done in 0.18 micron n-well CMOS technology using the Cadence Design Tools.

Team Member	Responsibility
Bi Pham	1st Mixer
Christina George	LNA
Derek van Gaal	2nd LNA+Image Rejection
Kevin Cheung	VCO
Mark Fairbairn	PLL
Vincent Karam	2nd Mixer

Table 1 Division of task for each group member

1.1 Front-end Mixer

The purpose of the Front-end Mixer was to upconvert the desired RF signal within the range of 50MHz to 850MHz to an IF frequency of 1.9GHz so that channel selection can be accomplished by subsequent filtering. This was done by mixing it with a tunable LO signal. By using an upconversion mixer at the front-end, the image rejection problem was reduced by relaxing the front-end filtering. The fractional tuning range required for the LO was also reduced simplifying the LO design.

The mixer must be able to handle the high signal power level coming out of the first LNA and hence, it must have high linearity with a low Noise Figure. There are tradeoffs with having high linearity and gain, the power consumption and noise of the circuit will also increase.

1.2 Specifications

The front end upconverting Gilbert mixer must be able to handle the power from the different signals coming from the 1st LNA. It should not consume too much current and have an acceptable noise figure. Therefore, the following specifications were set for the mixer.

- Total Current < 25mA
- Vdd = 3.3V
- IIP3 > 25 dBm
- Gain 0 to 4 dB
- Noise Figure (1st LNA & Mixer) < 10dB

1.3 Design Flow

The design and testing of the First Stage upconverting mixer will all be done using the Cadence Design Tools. Based on the mixer design criteria listed, a rough calculation will be made to set the DC bias operating points and obtain transistor parameters. The circuit will then be designed and simulated and DC values properly readjusted to improve results. Measurements will be made for the following characteristics: gain, 1dB Compression point, 3rd order intercept point and noise figure. The circuit will then be redesigned if it can not meet the specification. This will be followed by layout design implementation.

2.0 Mixer Theory

Mixers are used for frequency translation, they convert the RF frequency to the IF frequency by multiplying it with the LO frequency. This is shown in the result in figure 2. The mixing result

produces two signal located at the LO+RF and LO-RF frequency. One signal is the wanted IF signal and the other is the unwanted signal as shown in equation 1.

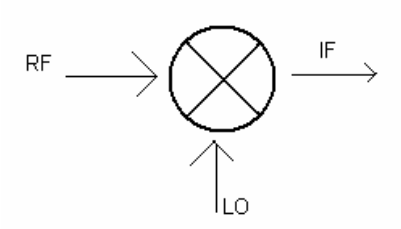


Figure 2 Mixers are frequency translator

$RF = A\cos(?_{RF})t \qquad LO = B\cos(?_{LO})t$

$IF = A\cos(?_{RF})t * B\cos(?_{LO})t = 1/2 * AB\,[\cos(?_{LO}+?_{RF})t + \cos(?_{LO}-?_{RF})t] \qquad (1)$

2.1 Mixers in Integrated Circuits

IC Mixers generally have a gain stage, a switching stage, and a differential IF output such as the one shown in figure 3. The current in the RF frequency is amplified by the gain stage at the bottom of the circuit. The current is then steered to one side of the output or the other depending on the value of the LO. The result is a mixing of the LO and RF frequencies.

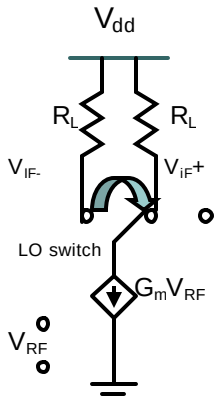


Figure 3 Simple Conceptual schematic of a mixer

2.2 Linearity

Linearity describes the region of operation where the output signal varies proportionally to the input signal. There are several ways to measure the linearity of a circuit.

1-dB Compression Point: In a real device, the input and the output power is linear only to a certain point. The 1dB Compression Point measures this point where the output power level is 1dB less than it would have been if it were an ideally linear device.

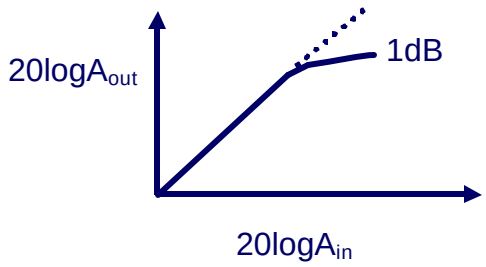


Figure 4 Definition of the 1-dB compression Point

Third Order Intercept Point (IP3): This is a theoretical point at which the fundamental and third order response intercepts. This point is found when two signals that are very close in frequency are applied to the mixer. Third-order intemodulation (IM3) appears at the output. The IM3 components will be at $2f_1 - f_2$ and $2f_2 - f_1$ which is in the vicinity of the desired frequency causing intermodulation distortion.

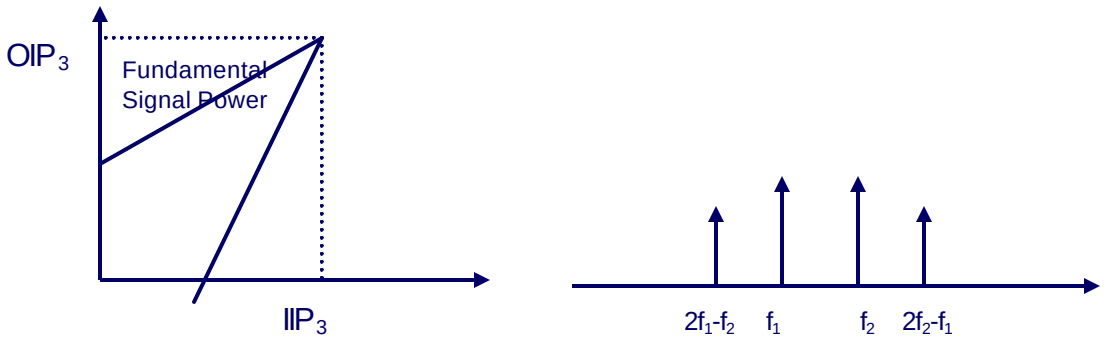


Figure 5 Definition of Third Order Intercept Point

1-dB compression and the third order intercept point are related to each other. By knowing one, the other can be approximated. For a single tone input, the 1dB compression point is about 9.66dB below the intercept point. For a two tone inputs, the ratio is larger by a factor of 5.25 or 14.4dB [3].

2.3 Conversion Gain

The voltage conversion gain of a mixer is defined as the rms voltage of the signal at the IF frequency divided by the rms voltage of the signal at the RF frequency. The gain can be approximated as following.

$$Vr_f = Vr_f \cos(v\, r_f * t)$$
$$V_o = Vr_f * V_{LO(t)}$$
$$V_o = g_m R_L(\frac{4}{p})[\frac{1}{2}\cos(w_{rf} - v_{LOz})t + \frac{1}{2}\cos(w_{rf} + v_{LOz})t...]$$

$$\therefore \frac{V_o(t)}{V_{rf}(t)} \approx g_m R_L(\frac{2}{p}) \qquad (2)$$

Where g_m is the transconductance of the V-I converter.

The coefficient is 2/p rather than 4/p because the IF signal is divided evenly between sum and difference components.

2.4.0 Noise

Noise is defined as any random interference that is unrelated to the signal of interest. The different types of noise in all circuits are thermal noise from resistors and channel resistance of MOSFETs. Shot Noise which is associated with the transfer of charge across an energy barrier. Flicker Noise arising from random trapping of charge at the oxide-silicon interface of MOSFETs [5]. In addition, mixers also suffer noise from the thermal noise generated by the output resistance of the LO and noise contributed by the switching pairs.

2.4.1 Noise Figure

Noise figure (NF) measures how much the signal to noise ratio (SNR) of a signal degrades because of the added noise as it passes through the mixer. The NF of the mixer is defined as the total SNR at the RF frequency divided by the SNR at the IF frequency.

$$\text{Noise Figure} = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) \qquad (3)$$

2.4.2 Noise Figure of Cascaded Systems

In a cascaded system such as the one shown in figure 6, the total noise is the combined noise contribution of each stage divided by the total available gain between the stages. It is dependent on the gain of subsequent stages because noise becomes less important once the signal has been

amplified. Therefore, the system noise figure (NF) is dominated by the noise performance of the first couple of stages of the system. The total noise factor is the sum of these individual contributions

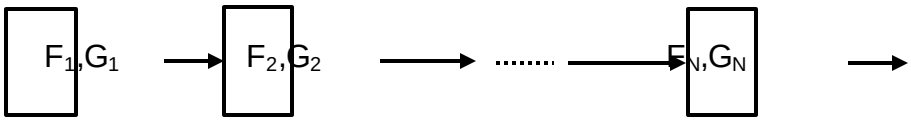


Figure 6 Cascaded systems for noise figure computation

Noise factor of the system.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{\prod_{n=1}^{N-1} G_n} \qquad (4)$$

$$\textit{Noise Figure (NF)} = 10\log(F) \qquad (5)$$

Noise figure, for a mixer, considers only the noise associated with the IF (f_{LO}-f_{RF}) frequency, according to the IEEE's NF definition for mixers, it assumes that there are no noise contribution at the image frequency ($2f_{LO}$-f_{RF}) due to mixing.[4] For the cable tuner, an Image Reject Filter preceding the mixer will remove the noise at the image frequency.

2.4.3 Noise Figure Requirement for the Mixer

In the specification, a noise figure for the 1st LNA and the mixer must be less than 10dB as the requirement. This NF also takes into account the image reject filter (Refer to figure 1) which removes approximately 3dB from the total noise figure. To calculate the maximum noise figure

allowed for the mixer and still meet the specification, it was assumed that without the filter, the total noise figure requirement would be less than 13dB (3dB will be removed from the filter). Therefore, equation (4) can be rewritten in terms of F_2 (mixer noise factor) and F_1 (LNA noise factor). The LNA was assumed to have a noise figure of 3dB with a gain of 12dB. The total noise factor for the LNA and mixer is 20 (13dB). Therefore, using equation xx, the noise figure of the mixer should be less than 18.6dB.

$$F_2 < G_1 F_{total} - G_1 F_1 + 1 \qquad (6)$$

$$F_2 < 4 \cdot 20 - 4 \cdot 2 + 1$$
$$F_2 < 73$$

Therefore, $NF_2 < 18.6dB$

3.0 Mixer Topologies

3.1 Active and Passive mixers

Passive mixers have higher linearity and better frequency response however; they do not have any gain and hence are not widely used in RF systems. Active mixers on the hand generally have gain thus reducing noise contributed by the succeeding stages.

3.2 Single-Balanced and Double Balanced Mixers

A mixer with a single-ended RF signal is called a single-balanced mixer. An example is shown on figure 7. This configuration is rarely used because it is more susceptible to noise in the LO signal. Its main drawback is the LO-IF feedthrough. That is, the LO signal could leak into the IF if the IF is not much lower than the LO frequency. The low pass filter following the mixer may not properly suppress the LO signal without affecting the IF signal [5].

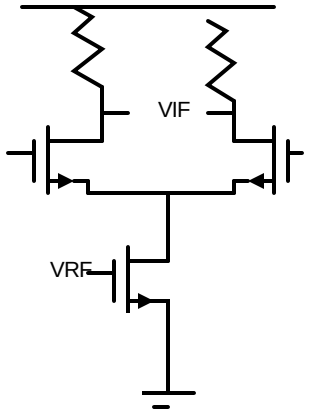


Figure 7 A single-balanced Mixer

Double Balanced Mixers are used to prevent the LO products from reaching the output. It is essentially two single-balanced circuits with the RF transistors connected in parallel and the switching pair in anti-parallel. Therefore, the LO terms sum to zero and the RF signal doubled in the output. This configuration provides a high degree of LO-IF isolation easing filtering requirements at the output [7]. Double Balanced mixers are less susceptible to noise than the single-balanced mixers because of the differential RF signal. Figure 8 shows a double balanced mixer, it is also known as the Gilbert Cell Mixer.

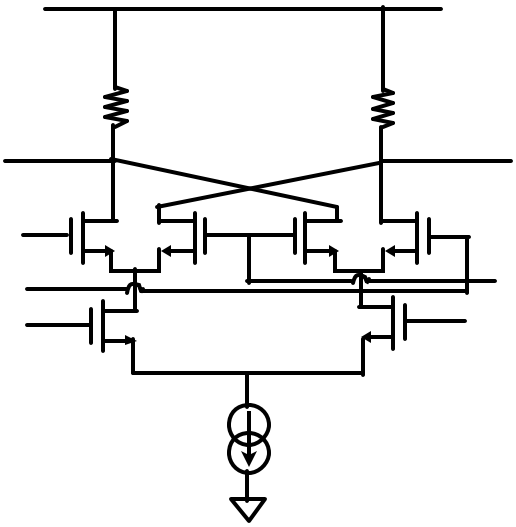


Figure 8 A Double Balanced mixer

3.3 Source Degeneration

An important mixer requirement is linearity. There are several ways to increase linearity such as increasing the voltage supply or increasing the current. However, the most common and effective method to improve linearity is to use some type of source degeneration. Figure 9 (a) shows the mixer with source degeneration resistors and 9 (b) with source degeneration inductors. Resistors are used when the size of the circuit needs to be minimized. Inductor degeneration is usually preferred because it has no thermal noise to degrade the noise figure, and it saves headroom because there is no voltage drop across it. In the design, resistor degeneration was used because the circuit must operate over a broad bandwidth.

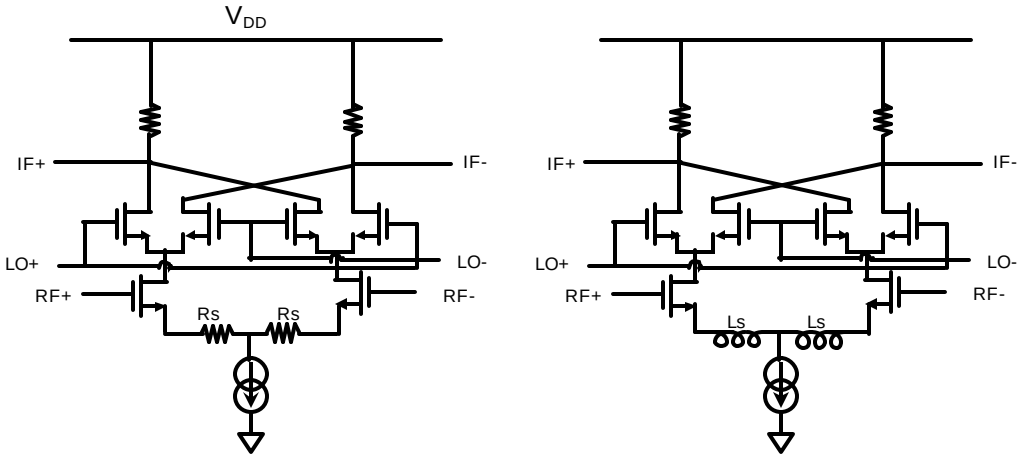


Figure 9 (a)Source Degeneration Resistors (b) Source Denegeration Inductors

4.0 Gilbert Cell

The Gilbert Cell has two pairs of transistors connected in parallel; this provides a double balanced mixer which attenuates the feed-through RF and LO components produced by the mixer. When two signals are mixed, the output will be the wanted frequency (the mixing) and the feed-through. Some of the feed-through is cancelled out due to a 180 degrees phase shift.

The two transistors with the RF terminals act as an amplifier increasing the gain of the signal before mixing. Two resistors, called emitter degeneration resistors, are connected between them. It can be adjusted to increase or decrease linearity or gain. The output is taken at the difference between IF- and If+ shown in figure 9. No input and output impedance matching are required for the mixer since the input comes from the image reject filter which is also on the same chip. A filter with high input impedance will be added at the output of the mixer to filter out the unwanted high frequency produced.

The Gilbert Cell topology was chosen for the design of the upconverting mixer. It provides reasonable conversion gain (IF power output with respect to the RF gain input), good rejection at the RF and LO ports (attenuation between signal inputs at the RF and LO and its level as measured at the output port), and a differential IF output connection [2]

The gain of this mixer with source degeneration resistor, R_S, is approximately equal to

$$\frac{V_o(t)}{V_{rf}(t)} \approx \frac{2}{p}\left(\frac{R_L}{R_s + \frac{1}{g_m}}\right) \qquad (7)$$

4.1 Gilbert Cell Design Guideline

All the transistors are operated in the saturation region. This region offers the largest gain and also makes the current less susceptible to the changing voltage across the transistors. The large signal current equation for a MOSFET in saturation is shown in equation (8). Equation (9) is a simplified version used to simplify calculations by neglecting the channel modulation. The transconductance of a device is depended on W/L and V_{GS} as shown in equation (10).

$$I_{DS} = \frac{1}{2} U_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + l (V_{DS} - V_{DS,SAT})) \quad (8)$$

$$I_{DS} = \frac{1}{2} U_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (9)$$

$$g_m = u_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \quad (10)$$

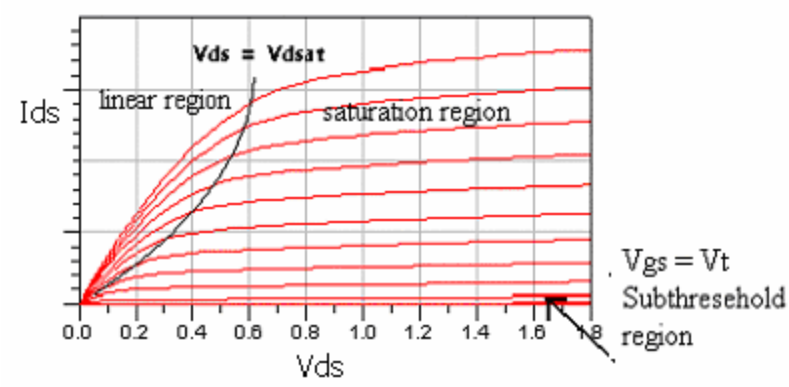


Figure 10 A Ids Vs. Vds plot showing the different regions of operation.

The condition for saturation is $V_{DS} = V_{GS} - V_T$ and $V_{GS} > V_T$ as shown in Figure 10

4.1.1 Gain Stage

The first stage mixer must have very high linearity to handle the power from the LNA. To help improve linearity, source degeneration resistors can be added just below the gain stage of the mixer. The transistors should be biased such that they have enough head room to swing without leaving the saturation region. The overdrive voltage (Vgs-Vt) should be around 200mV to 400mV. The gain of the mixer is proportional to *gm*.

Therefore, higher overdrive voltage means higher gain. Increasing W while keeping L at minimum also increases the gain. Increasing current also increases the gain as shown by the

equation (11). Decreasing the source degeneration resistor will increase the gain but decreases linearity.

$$gm = 2I_D / (V_{GS} - Vt) \qquad (11)$$

4.1.2 Switching Stage

When LO voltage level is too small the output voltage is dependent on the LO level, which means gain will be larger for larger LO because output voltage will become insensitive to the LO amplitude. Noise is also minimized for large LO. However, when the LO becomes too large, this leads to spikes in the signals, reducing switching speed and increase LO feedthrough [3]. The result of the spikes can also cause transistors to leave the saturation region. For complete switching, the LO level should be at least 100mV peak and at most 400mV peak.

When one transistor pair is conducting, we want the other pair to be completely off. If two pairs are conducting current at the same time, it will generate noise. Therefore, the overdrive voltage (Vgs – Vt) should be as close to zero as possible. This is the midpoint between turning the transistor on and off. Figure 11 demonstrates proper LO switching.

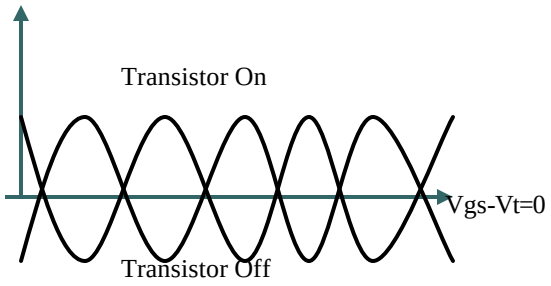


Figure 11 Illustration of proper LO switching

4.2 Fundamental Building Blocks

4.2. 1 Current Mirrors

Current mirrors are fundamental building blocks in analog circuits. They can be use to provide a current source to the circuit and also act as an active load at the output. An NMOS current sink was used to drive the mixer as shown in figure 12. Ideally, we want to replicate a small, reference current and scale it at M2.

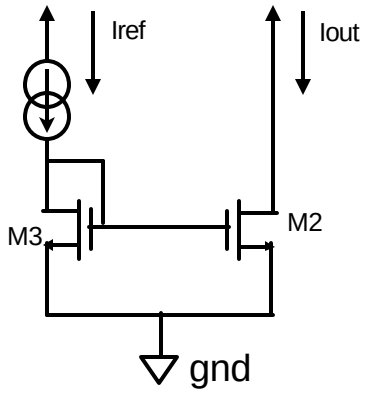


Figure 12 A simple NMOS current sink

Assuming both transistors are in the active region and neglecting channel length modulation for simplicity; we have the following equations.

$I_{DS1} = \frac{1}{2}u_nC_{ox}W_1/L_1(V_{GS1} - V_T)^2$ $I_{DS1} = \frac{1}{2}u_nC_{ox}W_2/L_2(V_{GS2} - V_T)^2$

And since the gates of both transistors are connected together and the sources grounded, we have $V_{GS1} = V_{GS2}$

Therefore, we have $I_{DS2}/I_{DS1} = I_{out}/I_{ref} = (W_2/L_2)/(W_1/L_1)$. *(12)*

This shows that by changing the ratios of W and L of each transistor, we can scale the current. In reality, I_{out} is not constant because M2 has a variable V_{DS}. As the Iout vs. V_{DS} plot shows, if V_{DS} varies, I_{out} varies with it and this can affect the biasing of the circuit. Therefore we want to design the current mirror so that I_{out} is less sensitive to the change in V_{DS}.

$$? I_{out}/I_{out} = ?(V_{DS2} - V_{DS1}) \qquad (13)$$

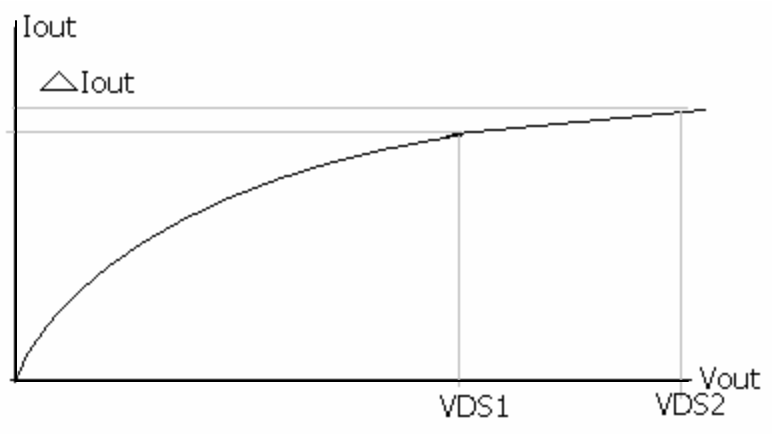


Figure 13 Graph of Iout Vs. VDS showing the changes in Iout when Ids changes.

4.2.2 Current Mirror Design Rule

The Length of devices is normally set equal to simplify the physical layout and to improve matching between the MOSFETs. The Length of M2 device (figure 12) affects the output resistance of the current mirror. We want it to have a high output resistance to make Ids less sensitive to Vds. Channel Length Modulation (?) decreases as the length increases and that ? is also inversely proportional to the output impedance as shown in the equation.

$$r_o = 1/ ?I_{DS} \qquad (14)$$

Therefore, we want to increase L so that ? would decrease. Generally, we want to keep L in the range of $2L_{min}$ to $5L_{min}$ [8]. L_{min} is the minimum length which is 0.18µm in this design technology. Circuit performance will deteriate if L is made large. Increasing L too much will lead to an increase in V_T, so V_{GS} must be made larger leaving less voltage headroom for the mixer. Since $Ids \propto (\frac{W}{L})$, to keep the current constant, W has to increase to compensate which leads to a large layout area [8]. Increasing L also increases V_T and this will result in less voltage headroom left.

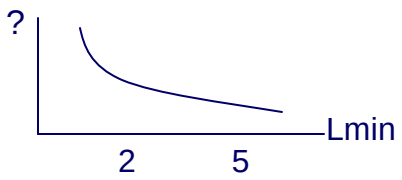
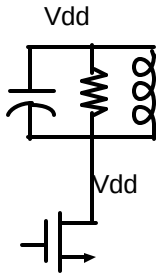


Figure 14 L should be between 2 and 5 times Lmin.

We want to choose Vgs such that we remain in the saturation region. If Vgs is too small, as seen in the current equation, Vgs-Vt will be approximately zero which means W/L has to be very large to compensate. If Vgs is too large, it will leave saturation entering the triode region if Vds is not large enough. This is because Vds > Vgs – Vt. A rule of thumb is to make Vgs slightly larger than Vt, a typical range would be from 200mV to 400mV larger. Vds should be in the range of Vd,sat+200mV to vd,sat + 400mV to ensure the device is in saturation even with the ac current swings. [6].

4.2.3 Tuned Load

The upconverting mixer has a broadband input and a fixed IF output. It only needs to provide gain over a narrow frequency range centered on the IF frequency. If headroom is a problem, a tuned load shown in figure 15 can be used to provide larger output swings. At DC, the inductor is shorted and hence there is no voltage drop across the tuned load so there is more room to work with. At the resonating frequency of the tank, the gain becomes gmR since the inductor and capacitor are an open circuit at this frequency.



Resonating Frequency ?o and the 3dB bandwidth

$$w_0 = \frac{1}{\sqrt{LC}} \qquad (15)$$

$$B = \frac{1}{CR} \qquad (16)$$

Figure 15 A tuned Load on a Mixer

5. 0 Design Approach

In the initial design, the Gilbert Cell with source degeneration resistors was chosen as the mixer topology.

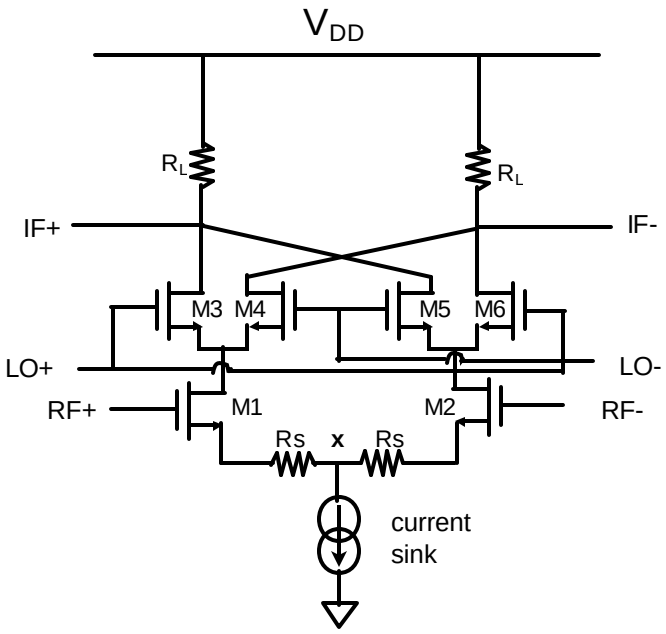


Figure 16 Gilbert Cell Mixer

The model file used in the design is the BSIM3 model file (t29b_mm_non_epi_params.txt) and the values for the models are shown in table 2.

K =UnCox/2	171.4uA/V^2
Vt	0.7V
V_{th0}	0.51 volts
Ids	3mA
Iout (Iss)	6mA

Table 2 Values used in the calculations

A current sink of Iss = 6mA was chosen to drive the mixer. Therefore 3mA of current is split between the differential pair. A voltage of 0.4V was chosen at node *x* shown in Figure 16 to keep the current sink operating in saturation. To preserve headroom, Rs was chosen such that there is only 0.1V drop across the resistor. To prevent compression at the IF, a voltage of

2.5V was decided on at the IF. From this decision, the load resistance was calculated to be 266.7Ω

$$Rs = \frac{V}{i} = \frac{0.1V}{3mA} = 33\Omega \qquad R_L = \frac{V_{DD} - V_D}{i} = \frac{3.3V - 2.5V}{3mA} = 266.7\Omega$$

5.1 RF stage

The gain is proportional to the transconductance of the RF pairs as shown in equation (17).

$$gm^2 = 2m_n C_{ox} \frac{W}{L} I_{DS} \qquad (17)$$

By knowing the required transconductance *(gm)*, the value for W can be determined. Using the gain equation (7), the *gm* of the RF gain stage transistors can be calculated. Hence, the widths can be found as followed.

$$Gain \cong 4dB \cong 1.82V/V$$

$$gm \approx \left[\frac{2}{p}\frac{R_L}{Gain} - R_S\right]^{-1} = 16.6m\Omega^{-1}$$

$$W_{1,2} = \frac{gm^2 L}{2m_n C_{ox} I_{DS}} = 27.4mm$$

The chosen overdrive voltage (Vgs-Vt) was 300mV. Therefore Vg =Vs+Vt+300mV = 0.5V+0.7V+0.3V = 1.5V

Let Vds = Vds,sat + 1V = 1.3V. Therefore, Vd = 1.8V

Two resistors were used as a voltage divider to bias the voltage at the gate. The resistors were chosen to be in the KΩs to minimize any current leakage into the gate.

5.2 LO stage

For proper switching, Vgs needed to be just slightly larger than Vt and W to be large.

Assuming Vt is 0.7V, Vgs was chosen to be 0.8V. Therefore, W is equal to 315um as shown below.

$$W = \frac{LI_{DS}}{K(V_{GS} - V_T)^2} = \frac{(180nm)(3mA)}{(171.4\text{uA/V2})(0.8\text{V} - 0.7\text{V})^2} \approx 315mm$$

Vg = Vgs + Vs = 0.8+1.8V = 2.6V

5.3 Current Sink

Vds_8 = 0.4V and Iss = 6mA were chosen as the values for the design refer to figure 17. To keep r_{o8} high, $L_{7,8}$ were chosen to be 540nm. $Vgs_7 = Vds_7 = Vgs_{8=} V_{th0}$+300mV = 810mV. A small current of 100uA was chosen for the reference current.

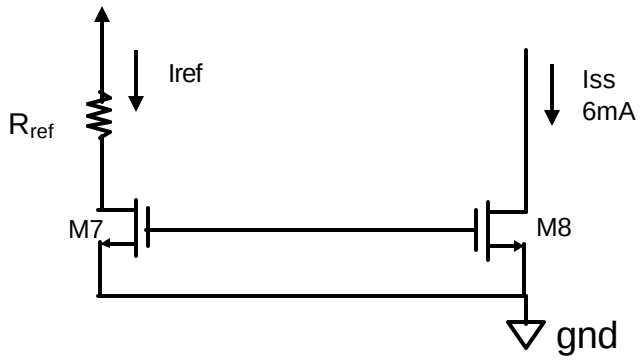


Figure 17 A current sink used to supply the current to the mixer

Therefore,

$$W_8 = \frac{LI_{ss}}{K(V_{GS8} - V_T)^2} \approx 210mm$$

Since $L_8 = L_7$ and $\frac{Iout}{Iref} = \frac{W_8}{W_7}$ W_7 was calculated to be $W_7 = \frac{W_8 Iref}{Iss} = 7mm$

$$Rref = \frac{V_{DD} - V_{DS7}}{Iref} = \frac{3.3V - 810mV}{100mA} = 25k\Omega$$

5.4 Parameters setup for initial Design

Parameters	Values
M1 width	27.4µm
M2 width	27.4µm
M3 width	315µm
M4 width	315µm
M5 width	315µm
M6 width	315µm
M7 width	7µm

Parameters	Values
M8 width	210
R_S	33 ?
R_L	266.7?
R_{ref}	25k?

Table 3 Values From The Calculations for Schematic in figure 16 and 17

These parameters were used to setup the initial design of the mixer and modifications were later made to optimize for the specifications outlined in section 1.2.

6. 0 Design Modification

Several modifications were made to the design after running the simulations for linearity and gain. The linearity achieved had an input IP3 of 5dBm which needed to be improved. Modifications were made to the widths of the gain stage transistors which were increased to improve gain. R_S was increased for better linearity, and more currents were also added. However, there were still linearity problems because of the small headroom. It was realized that to satisfy the requirement of a high linearity of 25dBm and a gain of 4dB several design modifications had to be made. More current was needed to drive the mixer for improved

linearity and gain, and tuned load was used to get more voltage headroom at the RF and IF ports. Since the design was well under the power consumption requirement, increasing more current was not a problem. Another advantaged of using a tuned load is that it can be designed off chip because the IF ports are connected to an off chip filter so the size of the mixer does not get larger.

A current sink of 20mA was chosen for this modification. If a MOS must drive a current of 20mA, its width would have to be very large making fabrication unrealizable. Therefore, two current sinks were used to provide 10mA each to M1 and M2 as shown in figure 6.0A. The degeneration resistor was connected between the two current sinks to improve linearity. This topology also helps headroom because there is no voltage drop across the degeneration resistor. A concern for using two current sinks to drive the mixer is if layout is not done properly there can be a mismatch which will increase the noise figure of the mixer.

7.0 Schematic

The finalized Gilbert Mixer is shown in figure 18 with resistors biasing the RF and LO ports. The component values are listed in table 4.

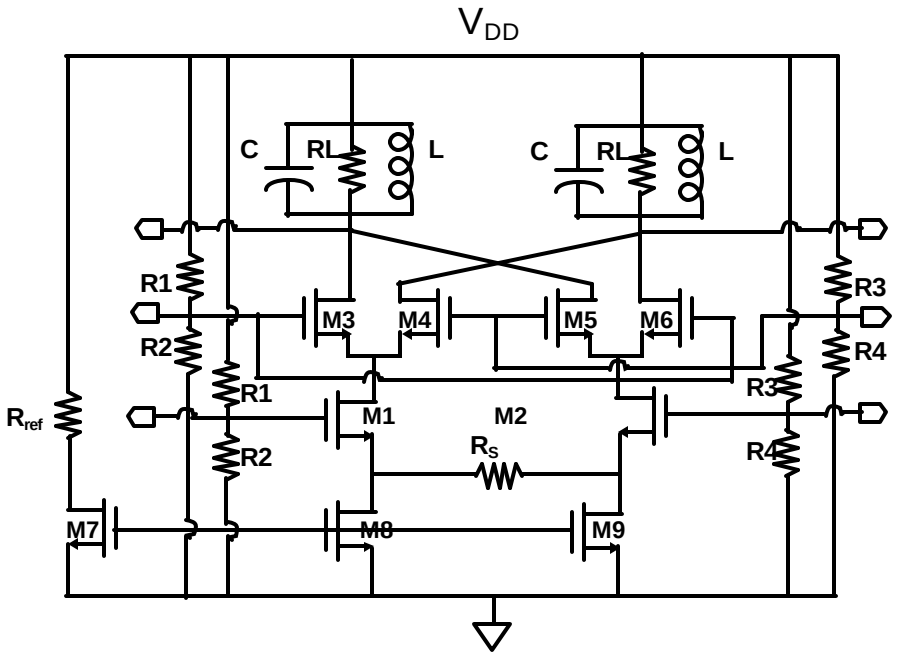


Figure 18 Gilbert Mixer Schematic with Bias Resistors

M1, M2 Width	100µm
M3, M4, M5, M6 Width	350µm
M7 Width	5µm
M8, M9 Width	200µm
R1	20 K?
R2	25 K?
R3	4 K?
R4	30 K?
Rs	150 ?
R_{REF}	8 K?
RL	700 ?
C	350pF
L	20nH

Table 4 Component Values of the Mixer with Bias Resistors

7.1 Schematic Simulation

The Gilbert mixer schematic is shown in figure 19. The testbench circuit used to simulate the mixer is shown in figure 20. The simulation was done using Spectre, a high speed and highly accurate analogue simulator from Cadence. The psin test ports were added to the RF, LO and

IF terminals to provide the input sources and to measure the output terminal of the circuit.

Table 5 shows the frequency and power level of the sources.

RF Frequency	50MHz
LO Frequency	1.95GHz
RF Power	0dBm
LO Power	-1.2dBm

Table 5 Frequency and Power Levels of Sources

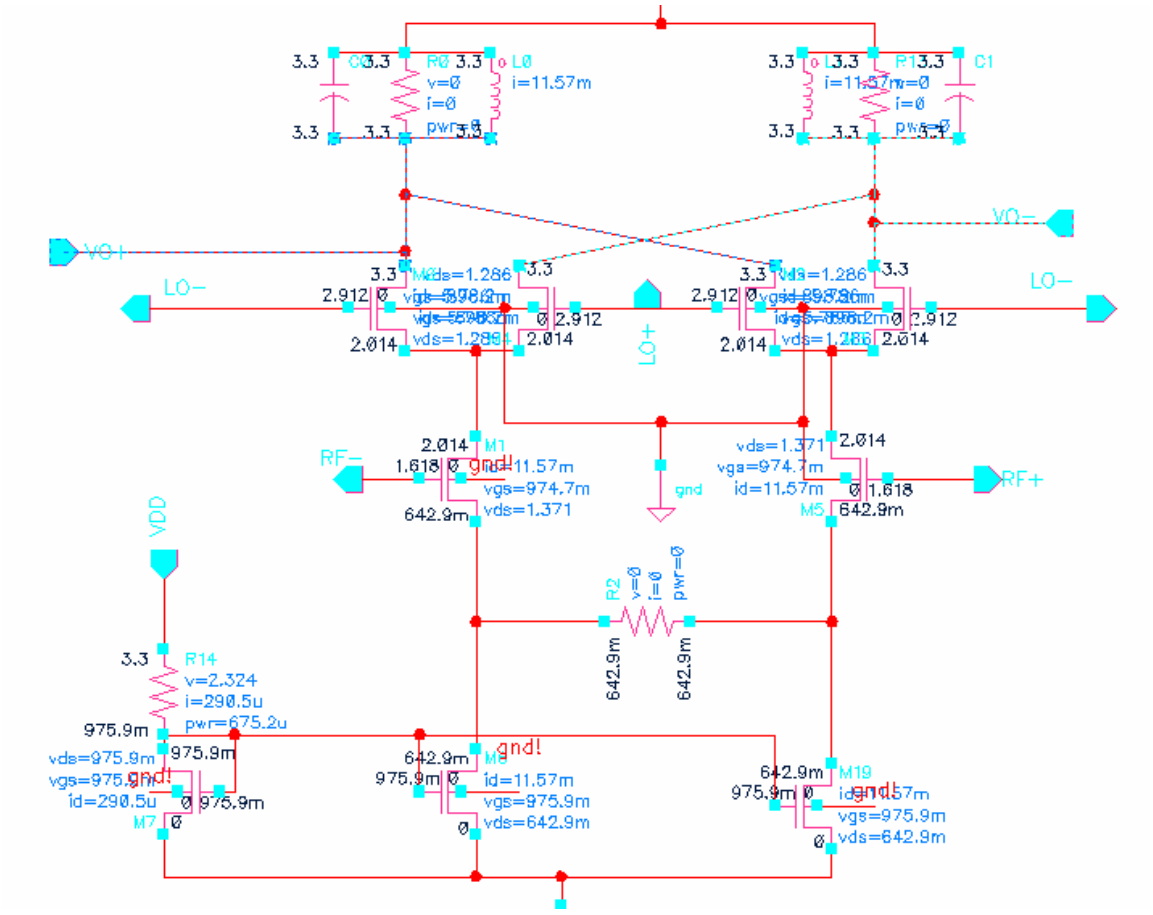


Figure 19 The Gilbert Cell Mixer Schematic View

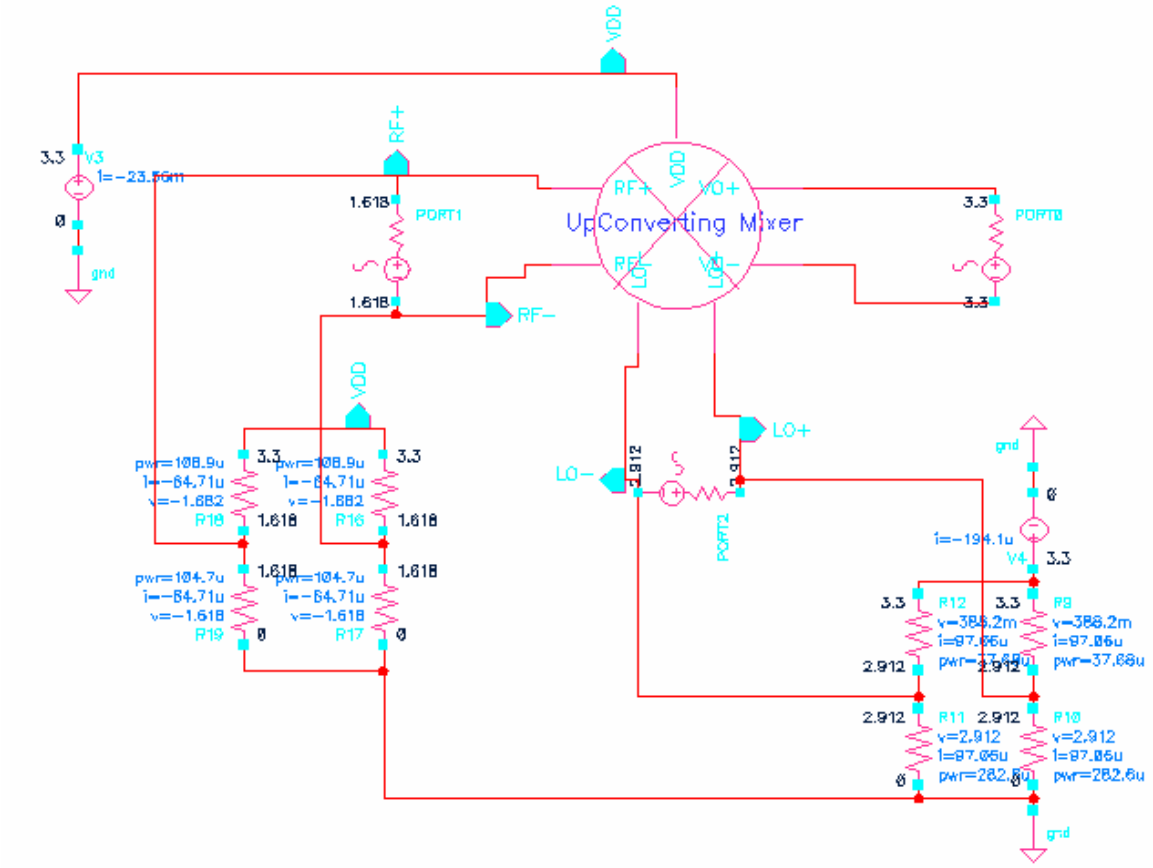


Figure 20 The testbench used to test the mixer and set the bias voltage at the input.

7.2 DC Analysis

The DC simulation was used to determine the proper DC operating point of the mixer circuit. It was used to verify that all transistors were operating in the saturation region. The gate, substrate and drain transconductances of the transistors were also provided from this simulation. Figure 19 shows the mixer with the DC operating point annotated on the circuit.

7.3 Transient Analysis

The Transient simulation was used to find the transient response of the circuit when the A.C. signals (RF and LO signals) are applied to the mixer. When the RF and LO signals are mixed, the result is a signal at the IF output located at 1.9GHz. Figures 21 and 22 show the time

varying input signals of the RF and LO and figure 23 shows the upconverted IF signal as a result of the mixing.

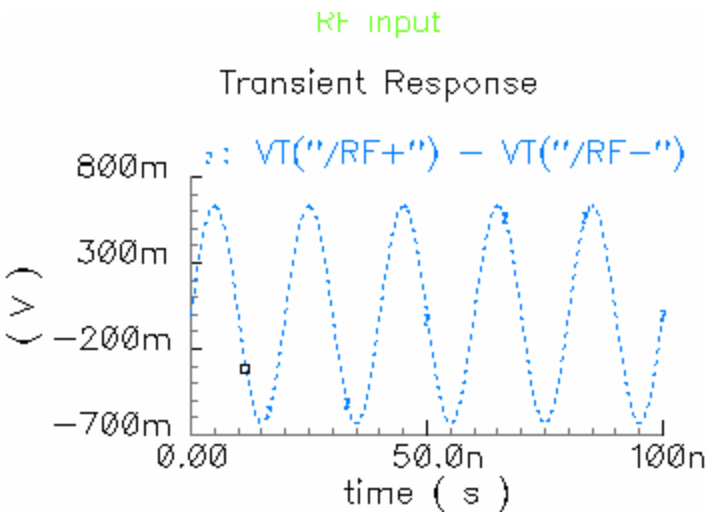


Figure 21 The RF signal located 50MHz

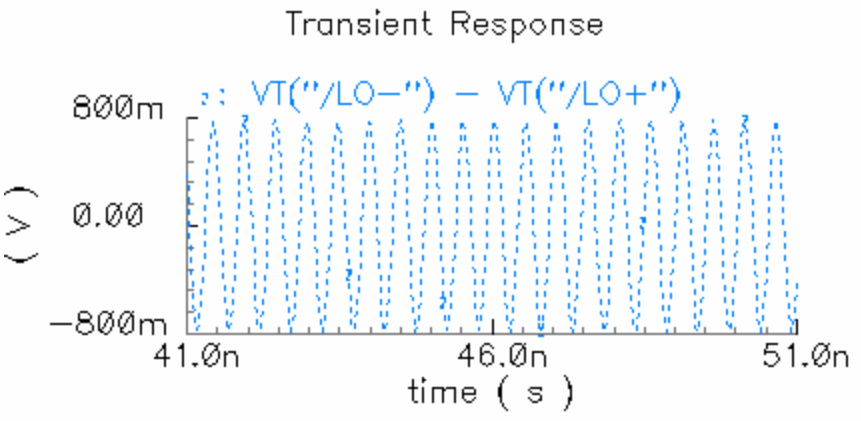


Figure 22 The LO signal located at 1.95GHz

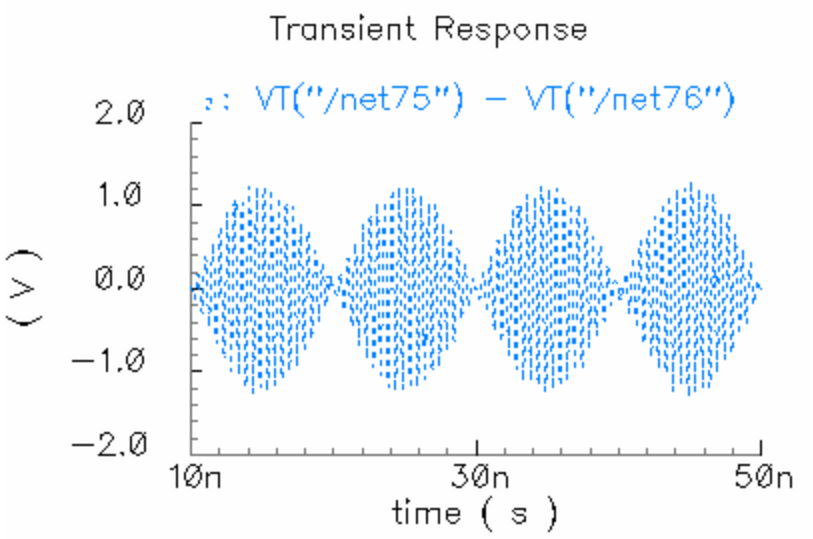
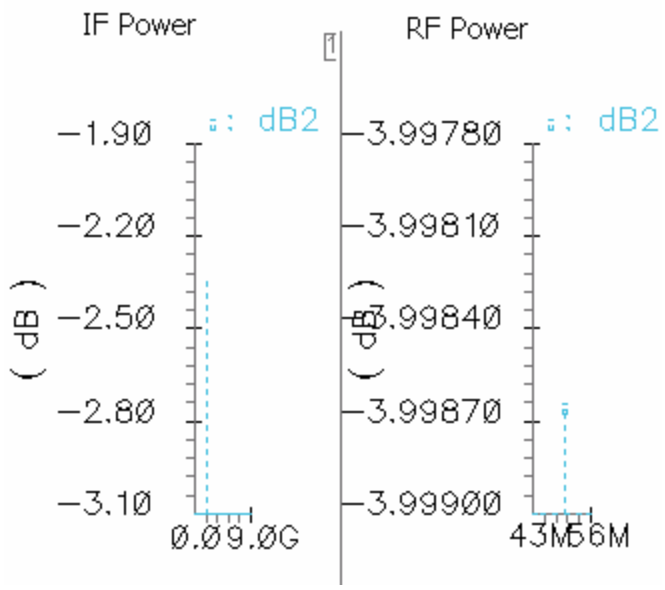


Figure 23 The IF signal at 1.9GHz resulted from the mixing of the IF and LO

The voltage conversion gain of the mixer was determined by doing a DFT at the differential input and output ports, and the power level were plotted as shown in figure 24. The voltage conversion gain is the difference between the input and output power and hence is equal to 1.65dB.



(a) **(b)**

Figure 24 (a) The output power at 1.9GHz is -2.35dB. (b) The input power at 50MHz is -4dB

7.4 Periodic Steady State (PSS) Analysis

This is a large signal analysis that computes the periodic steady-state response of a circuit. This simulation was used to find the linearity of the circuit by finding the 1dB and the IP3 compression point. To find the 1dB compression point, the input RF power was swept from 8dBm to 16dBm. The plot is shown in figure 25.

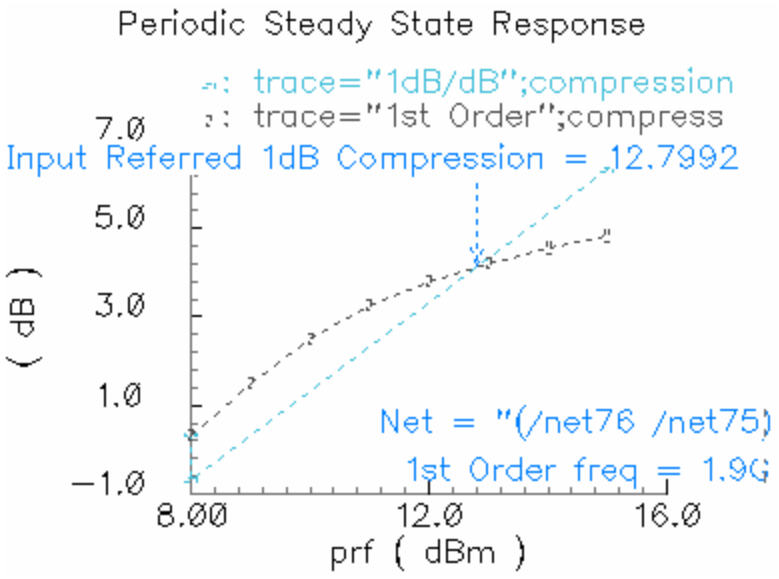


Figure 25 The 1dB compression point plot

The 1dB compression point occurred at 12.8dBm (input referred). A quick approximation for the IP3 point would be 22.46dBm (12.8dBm+9.66dBm).

To simulate for the IP3 point, two signals (50MHz and 60MHz) were applied to the mixer and the power of the signals were swept for the same range during the PSS analysis. The result is shown in figure 26. The simulation indicated that the input IP3 is at 20.46dBm. The IP3 simulation should never be swept passed the 1dB compression point which can lead to oxide-breakdown in the transistors because of the high gate voltage.

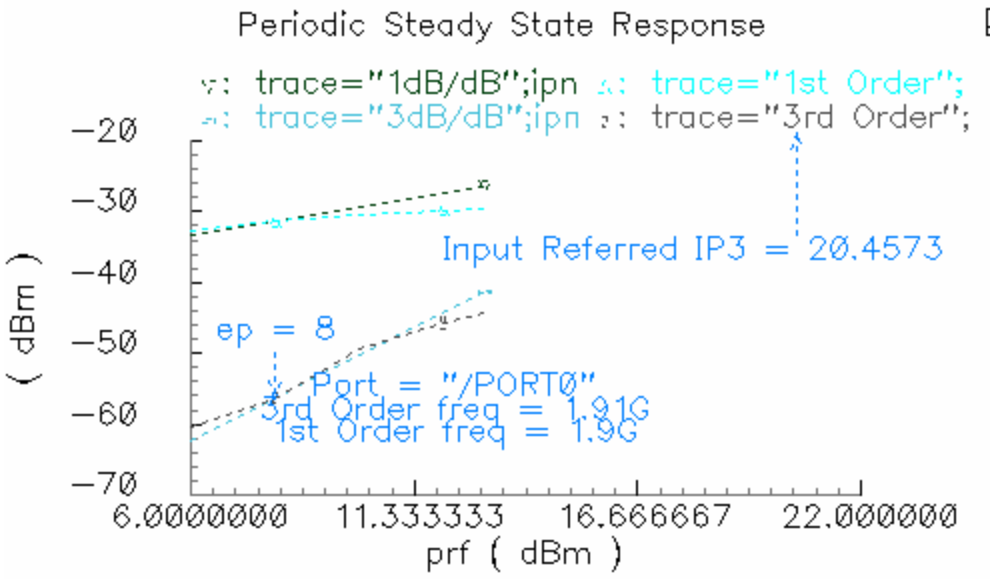


Figure 26 IP3 simulation of the mixer

7.5 Pnoise analysis

This simulation computes the total noise at the output, which includes contributions from the input source and the output load. It is used together with the PSS analysis to determine the mixer's single sided noise figure 27. The analysis includes the effects of noise folding, aliasing and frequency conversion effects. The single sided noise figure of the mixer at 1.9GHz is 17.2dB.

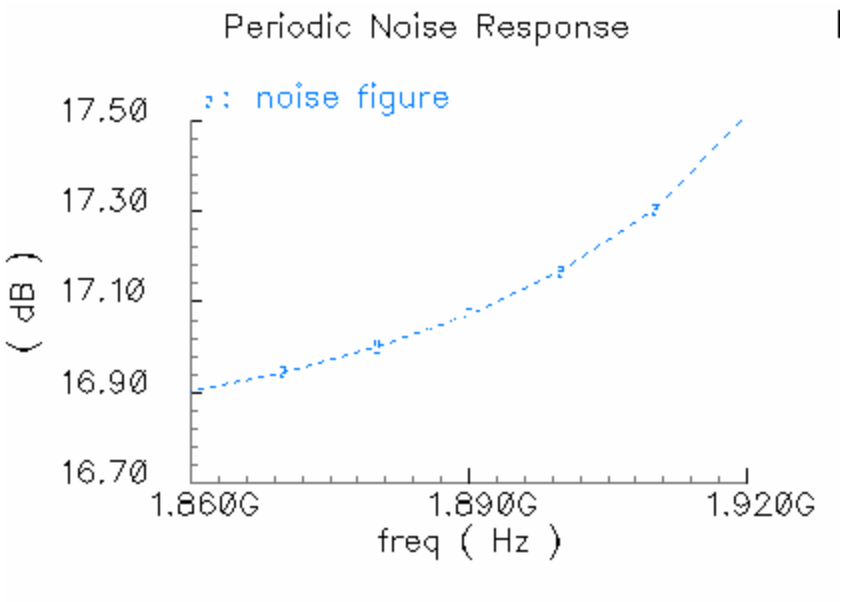


Figure 27 Single Sided noise figure of the mixer at 1.9GHz

7.6 Design Summary

The performance of the mixer is summarized in Table 6. To get the power consumption, the total current used by the mixer was multiplied by the voltage supply of 3.3V. The total noise figure of the 1st LNA and the mixer was calculated using equation (4). The result of the simulation for the IIP3 showed that it was slightly lower than the linearity requirement in the specification. With an exception to the IIP3, the mixer design met all the specification outlined in section 1.2.

Mixer Performance	Design Specification	Simulation Result
Voltage Power Gain	0 to 4dB	1.65dB
Input Third Order Intercept Point (IIP3)	25dBm	20.45dBm
Power Consumption	< 82.5mW	77.7mW
Total Current	< 25mA	23.56mA
Noise Figure (1st LNA + Mixer)	< 10dB	8.6dB
Noise Figure Mixer	< 18.6dB	17.2dB

Table 6 Mixer Performance Summary

8.0 Layout Overview

Layout defines the geometries of the integrated circuit that appear on the masks used in fabrication. The geometries include n-well, active, polysilicon, n^+ and p^+ implants, interlayer contact windows, and metal layers. Figure 28 shows an example of a layout of an NMOS transistor. The layout of the mixer was done for fabrication in the n-well CMOS 0.18micron technology process. The software used for layout was Virtuoso which was part of the Cadence Design Environment.

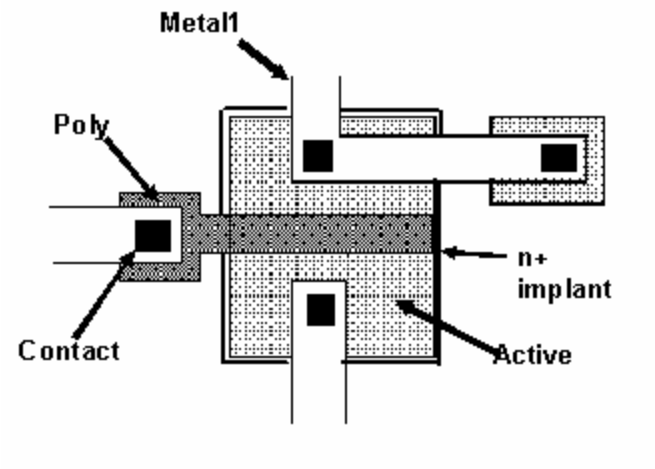


Figure 28 Layout of an NMOS transistor.

The mixer was laid out in sections, known as cells, and will be integrated together to form the complete mixer circuit. This modular design allows easy modification to the mixer by simply changing the cells without having to re-layout the whole circuit.

8.1 Design Rules

With an exception of the width and length of each transistor which is determined by the schematic design, the other dimensions in the layout are governed by a set of design rules associated with the 0.18µm technology process. Following these rules guarantees proper transistor and interconnect fabrication despite various tolerances in each processing step. [9] The main design rules are categorized as minimum: width, spacing, enclosure, and extension. All of which can be checked for violation by running a DRC (Design Rule Check) in Virtuoso. In addition, proper design techniques should be followed to minimize effects such as susceptibility to antenna, crosstalk, mismatches, and noises.

8.2 Antenna Effect

This occurs when the gate of a MOSFET is connected to a large piece of conductive material such as metal1 (Figure 29 (a)). During the etching process, the metal acts as an "antenna", gathering ions and rising in potential. This can lead to an increase in gate voltage leading to gate oxide breakdown, damaging the MOSFET. Large area interconnects are usually avoided if possible. However, a discontinuity can be created between the gate and the large area interconnects by adding another metal layer as shown in Figure 29 (b).

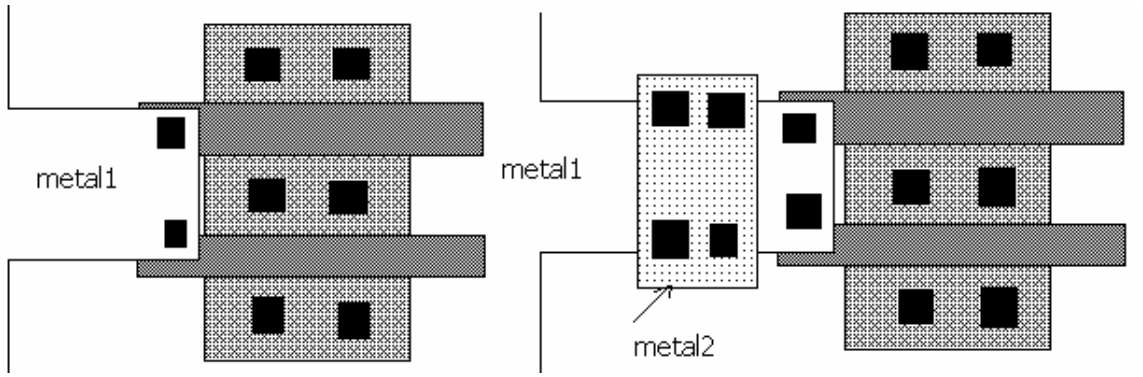


Figure 29 (a) Layout susceptible to antenna effect, (b) discontinuity in metal1 layer to avoid antenna effect

8.3 Multifinger Transistors

Large transistors are usually broken up into multiple small transistors called "fingers". This reduces both the S/D junction area and the gate resistance. However, too many parallel fingers can lead to increase in the capacitance associated with the perimeter of the source and drain regions. Generally, the width of each finger is chosen such that the resistance of the finger is less than the inverse of the transconductance associated with the finger [9].

8.4 Symmetry

Layout symmetry in the mixer circuit is important. Asymmetries in the RF differential transistors introduce input referred offsets which limits the minimum signal level that can be detected. A symmetric circuit suppresses the effect of common-mode noise and even-order nonlinearity minimizing any port-to-port feedthrough. The environment surrounding the devices must also be symmetrical to prevent mismatch between the devices because of the imperfection in the fabrication process.

8.5 Gain Stage

To prevent the effect of gradients resulting in mismatches between the differential RF pairs, a common-centroid configuration was used to reduce the effect of first-order gradient along both axes. As shown in figure 30, each transistor is broken into two halves and places diagonally opposite of each other and then connected in parallel. Different metal layers were used to make overlapping connections. Although attention was given to the routing of interconnects, capacitances from the wires to ground and between wires may increase slightly as a result of interconnect lines being close to each other. The width to length ratio of each transistor is 100um/0.18um. Each transistor has 16 gate fingers that are 6.25 microns long.

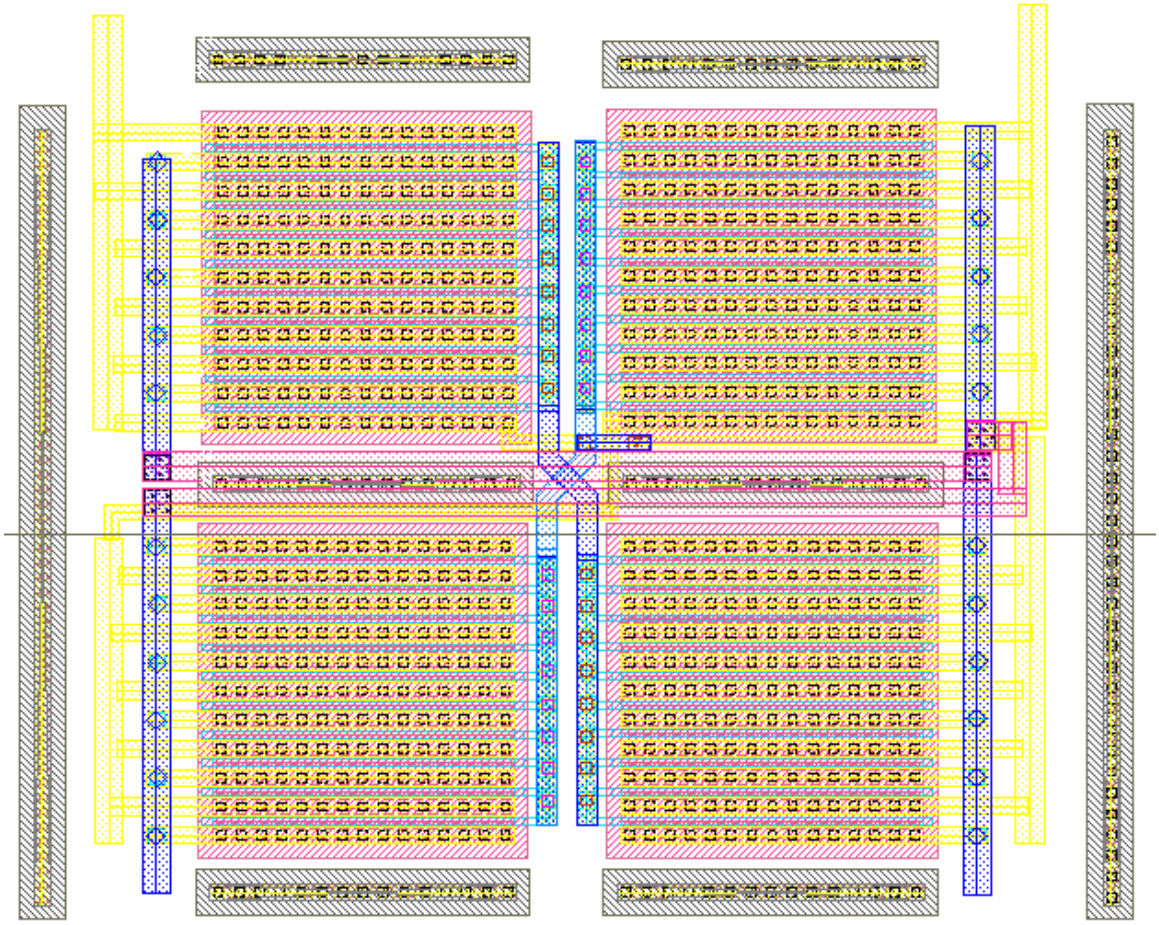


Figure 30 common-centroid configuration of the Gain Stage Differential Pair

8.6 Switching Stage

The transistors were laid out by interdigitating each differential pair. If the devices are represented by the letters A and B, then the arrangement was done in the form of AAAAAAAAAABBBBBBBBBBAAAAAAAAAABBBBBBBBBB. This ensures that all the transistors are identical and have the same capacitive parasitics. This setup also minimizes the interference between the pairs during switching. Each transistor is broken into 20 gate fingers. The ratio of W/L is 350um/0.18um. The layout of the differential switching pair is shown in figure 31.

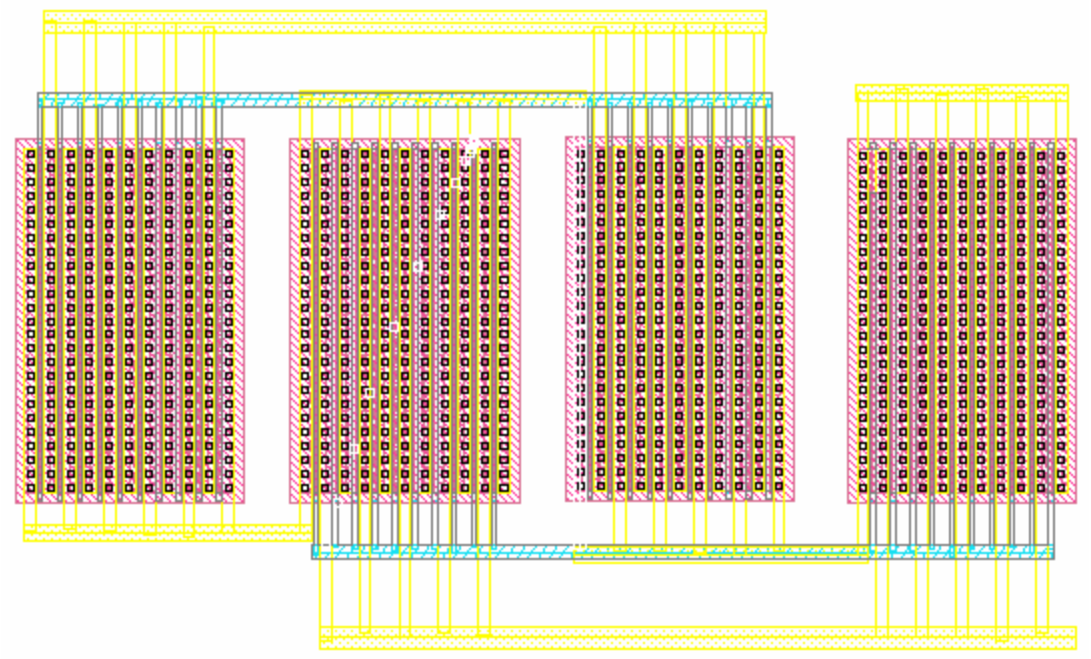


Figure 31 Layout of the differential switching pair

8.7 Source Degeneration Resistor

Resistors can be realized by many different conductors. In the layout, polysilicon was used to make the resistor because it has high linearity, low capacitance to the substrate, and relatively

small mismatches. [9] Figure 32 shows the layout of the source degeneration resistor. It has a resistance of 150 O and a size of 1.899 µm.

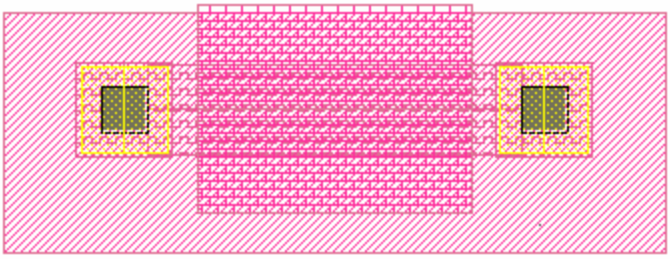


Figure 32 The layout of the Source Degeneration Resistor

9.0 Future Work

The design of the 1.9GHz Gilbert Mixer was, for the most part, very successful. Linearity was slightly lower than required, while all other mixer performances met the specification. Since this was a front end mixer, linearity was very important because it must handle all the power that comes from the LNA. Therefore, other performances of the mixer can be sacrifice in order to improve the linearity of the mixer. The source degeneration resistor can be increased to improve linearity although gain would decrease. If current consumption is not a big issue, more currents can be used to drive the mixer improving both linearity and gain.

In the future, work will be done to connect the separate cells laid out to complete the layout of the Gilbert Mixer. Layout will also be done to the current mirror design. This will allow for the mixer circuit to be extracted verifying its operation.

10 Conclusion

The 1.9GHz Gilbert Mixer is designed to be at the front end of a typical cable tuner. It upconverts the desired signal within the range of 50MHz to 850MHz to an IF frequency of 1.9GHz, so that channel selection can be accomplished by subsequent filtering.

The design of the mixer was done using models provided by the Cadence Design Environment. Simulation results showed that the mixer performance have met all of the specification with an exception to the IIP3 which is slightly lower than 25dBm. Improvement to linearity can easily be made by increasing current through the mixer, although power consumption will also increase. The layout of the mixer proved to be a challenge in the project because of the designer's lack of knowledge of layout processes. Although layouts of the main components of the mixer circuit were completed, they needed to be combined to form the mixer layout.

The toughest part of the project was to increase the linearity of the mixer. Several modifications to the design were made including the use of a tuned load before it was successful. However, as the understanding of the CMOS design increased via research and taking an analog integrated course, progress in the project was made faster. The designer is now confident that future CMOS design work can be performed in a much shorter time.

The experience from this project is relevant to the work done by IC designers in the high tech industry. The learning experience gained from this project has given the designer more confidence and interest in the area of analog CMOS design. In addition, the designer hopes

that the research and work done in this project will also help others in the designs of CMOS mixers.

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