Low Frequency gain = $\frac{v_o}{v_i} = \frac{v_o}{v_z} \cdot \frac{v_z}{v_i} = A_o = g_{mo}R_o \cdot g_{mI}R_z$ $\frac{v_o}{v_i} \approx A_o \frac{\omega_{p2}\omega_{p2}}{z} \frac{(-s+z)}{(s+\omega_{p1})(s+\omega_{p2})}$

dominant pole = $\omega_{p1} \approx -\frac{1}{R_z g_{mo} R_o C_c}$ next pole = $\omega_{p2} \approx -\frac{g_{mo}}{C_L}$ RHP zero = $\omega_z \approx \frac{g_{mo}}{C_c}$

stability: p_2 and z must be beyond UGBW enough so total phase shift due to p_2 and z $< 45°$.

Rules of thumb: Gregorian and Temes $|p_2| = |z| = 3$ UGBW $\rightarrow 53°$ phase margin

Allen and Holberg: $|z| = 10$ UGBW, $|p_1| = 2.2$ UGBW $\rightarrow 60°$ phase margin

UGBW $= \frac{g_{mI}}{C_c}$, Slew Rate = $\frac{I_3}{C_c}$, Increased load capacitance reduces stability since p_2 moves to lower frequency.

Additions to Pole Splitting: The zero in the RHP can result in instability. Can remove, or compensate for with feedback buffer, or resistor in series with C_c.

Buffer, typically source follower, to allow feedback only (removing feed forward) This removes the zero, and the system is left with two poles. These should be separated by the DC gain, or more for stability.

Series Resistance adds $\omega_{p3} = -\frac{1}{R_c C_c}$, changes ω_z to $\omega_z = \frac{1}{\left(\frac{1}{g_{m6}} - R_c\right)C_c}$, this allows one to move $\omega_z \rightarrow \infty$, or bring it into the LHP where it can cancel out ω_{p2} approximately**.**

Offsets for opamp gain A: $V_{i,off} = \frac{V_{o,off}}{A}$**.**

Gain Error with Feedback: For high A, $\frac{v_o}{v_i} = \frac{1/B}{1+1/(AB)} \approx \frac{1}{B}\left(1 - \frac{1}{AB}\right)$, here, desired gain $\approx \frac{1}{B}$, Gain error= $\frac{1}{AB}$ where

AB = loop gain $\rightarrow$ Open loop gain in dB, Closed loop gain is $\frac{1}{B}$ in dB

Folded Cascode Amplifier

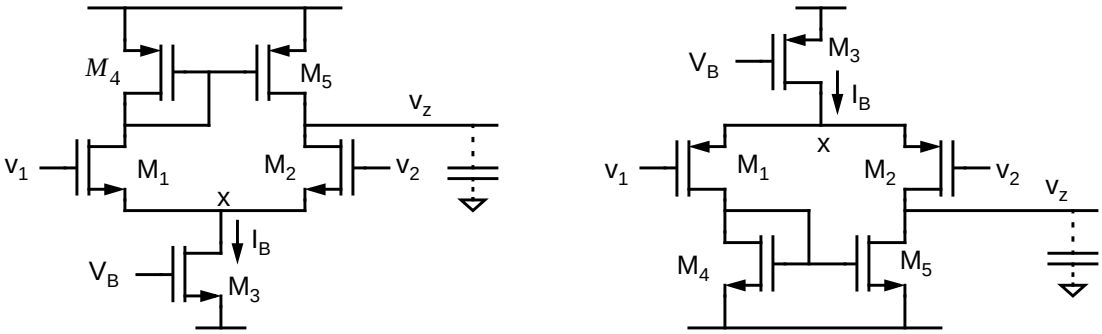
- single stage (output is directly $\frac{g_{mI}}{2}v_{in}$) high frequency capability - gain = $\frac{v_o^+ - v_o^-}{v_{in}^+ - v_{in}^-} = g_{mI}R_o$, typical gain about 1000 or 60 dB. R_o is high due to cascodes- Dominant pole, UGBW is set by load capacitance thus larger load results in more stability

Differential Pair with Resistors sm. sig: $g_{m1} = g_{m2}$, $r_{eq} = R \| r_o$, where $r_o = \frac{1}{g_o}$ of M_2.

$v_{o2} = \frac{g_{m1} r_{eq}}{2}(v_1 - v_2)$, $v_{o1} = -\left(\frac{g_{m1} r_{eq}}{2}\right)(v_1 - v_2)$.

Common-mode gain $v_{o1} = v_{o2} \approx \frac{g_{o3}}{2} \cdot R \cdot v_C$, where $v_C = \frac{v_1 + v_2}{2}$.

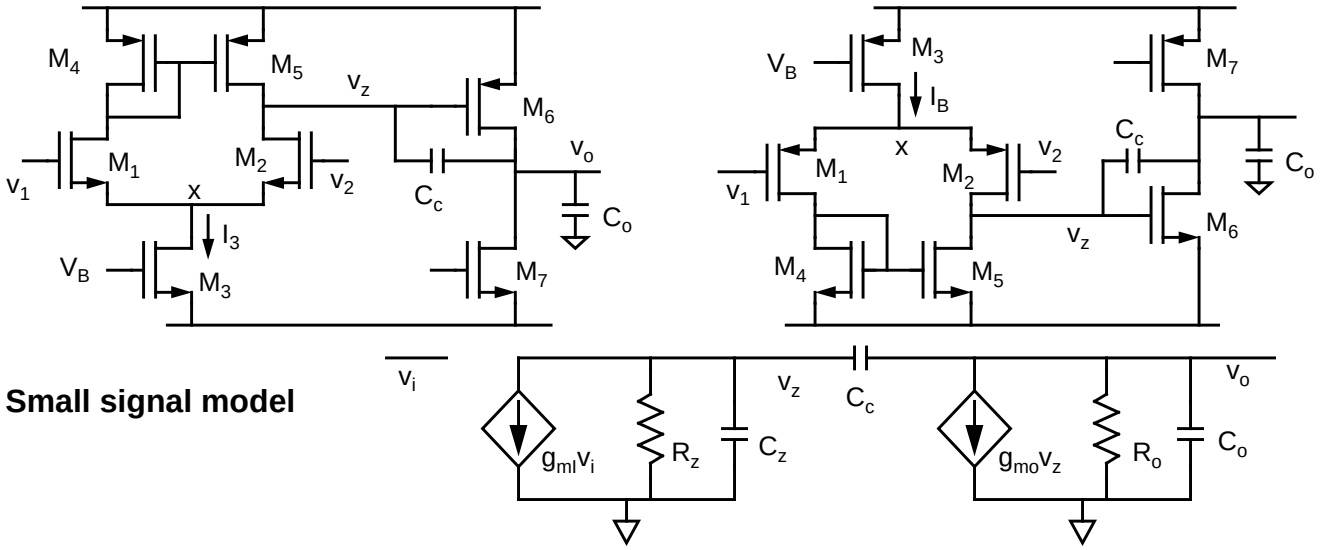
Differential Pair with Current Mirror Load



i_{r1} is mirrored to M_5 thus doubling output current and gain. difference mode gain $A_d = \frac{v_z}{(v_1 - v_2)} \approx g_m R_{eq}$, or $\frac{g_m}{g_{eq}}$,

where $g_{eq} = g_{o5} + g_{o2} = \frac{I_B}{2}(\lambda_2 + \lambda_5)$ common-mode gain $A_C = \frac{v_z}{\left(\frac{v_1 + v_2}{2}\right)} \approx -\frac{g_{o3}}{2(g_{m4} + g_{o4})}$, CMRR = $\frac{A_d}{A_c}$

Two-stage opamp with pole splitting compensationl

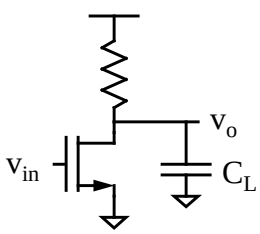


Small signal model

Where: $v_i = (v_{in^+} - v_{in^-})$, $g_{mo} = g_{m6}$, $g_{mi} = g_{m1} = g_{m2}$, $R_o = r_{o6} \| r_{o7}$, $C_z =$ =parasitic cap, $C_o =$ load cap.

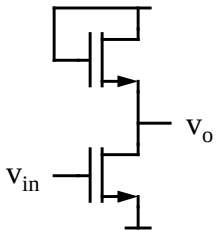
Exact Gain is: $\frac{v_o}{v_i} \approx -\frac{g_{m1}}{C_L} \frac{(s - g_{m6}/C_c)}{s^2 + s\left[\frac{g_L}{C_L} + \frac{g_z}{C_c}\frac{(C_L + C_c)}{C_L} + \frac{g_{m6}}{C_L}\right] + \frac{g_z g_L}{C_L C_c}}$

Gain Stages (Shown with NMOS Drivers)



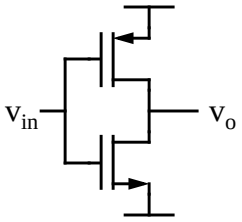
Resistive Load

$$\frac{v_o}{v_{in}} = \frac{g_m}{g_L + g_{ds}}$$



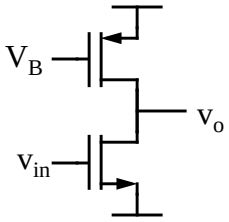
Diode Load

$$\frac{v_o}{v_{in}} = \frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}}$$



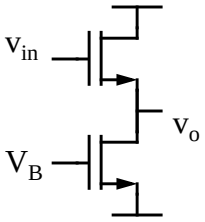
Digital Style

$$\frac{v_o}{v_{in}} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}}$$



Current Source Load

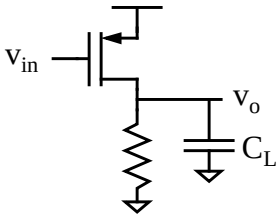
$$\frac{v_o}{v_{in}} = \frac{g_{m1}}{g_{ds1} + g_{ds2}}$$



Source Follower

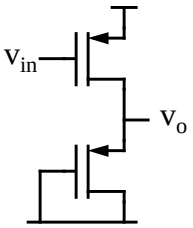
$$\frac{v_o}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1}}$$

Gain Stages (Shown with PMOS Drivers)



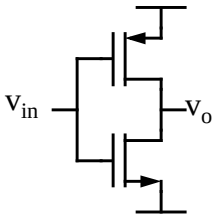
Resistive Load

$$\frac{v_o}{v_{in}} = \frac{g_m}{g_L + g_{ds}}$$



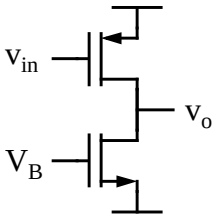
Diode Load

$$\frac{v_o}{v_{in}} = \frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}}$$



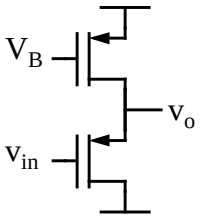
Digital Style

$$\frac{v_o}{v_{in}} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}}$$



Current Source Load

$$\frac{v_o}{v_{in}} = \frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

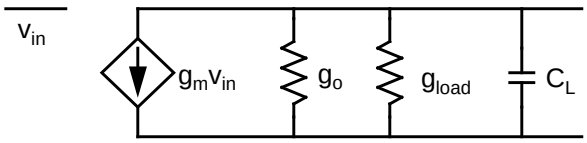


Source Follower

$$\frac{v_o}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1}}$$

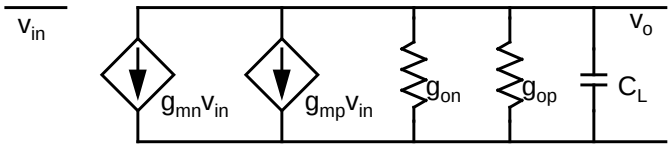
Small Signal Model

The gain of each, except for the last two is $\frac{g_m}{g_{eq}}$ where $g_{eq} = g_m + g_{load}$, and model is as below



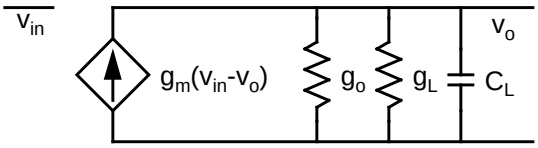
where g_{load} and C_L are determined by the load

Digital Style



low frequency gain = $\frac{(g_{mn} + g_{mp})}{g_{eq}}$

Source Follower

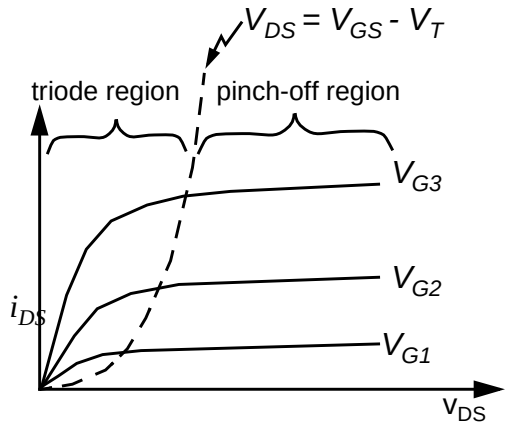


low frequency gain = $\frac{g_m}{g_m + g_{eq}} \approx 1$

Slew Rate . Use current into capacitor, calculate $i = C\frac{\Delta v}{\Delta t}$ where $\frac{\Delta v}{\Delta t}$ is the slew rate.

Pole Frequency. $\omega_p = \frac{1}{r_{eq}C}$ where $r_{eq} = \frac{1}{g_{eq}}$ Unity Gain Bandwidth: $UGBW \approx \frac{g_m}{C_L}$

Transistor Characteristics (N Channel)



Simple Square Law Equations

Triode: $I_{DS} = k_p \frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \quad V_{DS} < V_{GS} - V_T$

Pinch Off: n: $I_{DS} = \frac{k_p}{2}\frac{W}{L}(V_{GS} - V_T)^2 \quad V_{DS} > V_{GS} - V_T$

(use $|V|$ for pmos) $|I_{DS}|_p = \frac{k_{pp}}{2}\left(\frac{W}{L}\right)_p (|V_{GS}| - |V_T|)^2$

$K_{pn} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} = \mu_n C_{ox} \quad K_{pp} = \frac{\mu_p \varepsilon_{ox}}{t_{ox}} = \mu_p C_{ox}$

Channel Length Modulationt slope factor λ: $\frac{\Delta i_d}{I_D} = \lambda \Delta v_d, \quad \lambda \propto 1/L$.

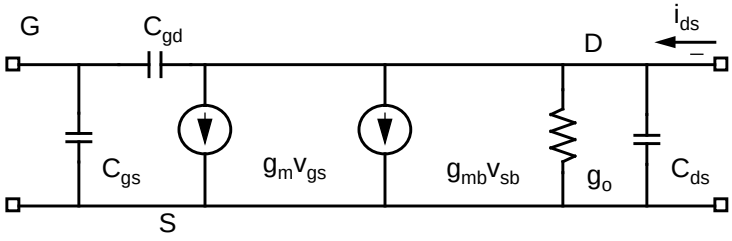
Transistor equations including channel length modulation:

Triode: $I_{DS} = K_P \frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}(1 + \lambda v_{DS})$ Pinch Off: $I_{DS} = \frac{K_P}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda v_{DS})$

Body Effect γ - nonzero V_{SB} changes the threshold voltage as:

$V_T = V_{T0} + \gamma[\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}]$ typically $2|\phi_F| = 0.7$ V Result: threshold is increased

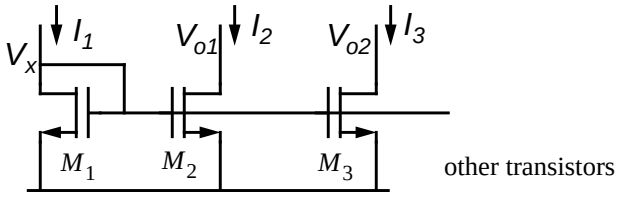
Small Signal Parameters in Pinch-Off



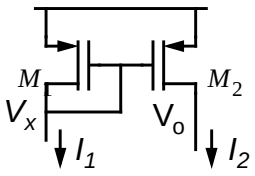
$g_m = \frac{di_{ds}}{dv_{gs}} \approx \sqrt{2k_p \frac{W}{L} I_{DS}} = k_p \frac{W}{L} v_{on}$

$g_o \approx I\lambda \qquad \lambda \propto \frac{1}{L}$

Diode Connection and Current Mirrors: Diode Connection: as M_1 below, connect drain and gate, hence $V_{DS} = V_{GS}$, if $V_{DS} > V_T$, then always in pinch off. Small signal model with $g = g_m + g_o$.



other transistors



Cuurent Mirror: $I_2 = I_1$ if $V_{o1} = V_x$.Otherwise currents will not match exactly because of output impedance e.g., at V_{o1} it is given by r_o of M_2. Can increase by using cascode or other types of mirrors.