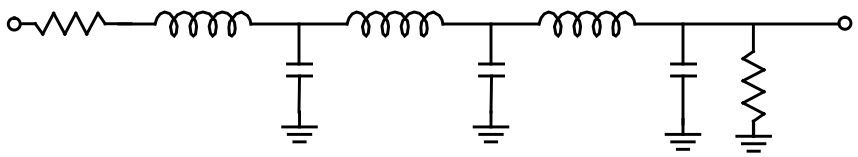
Integrated Filters

Historically, filters used R,L, C, e.g.,



discrete inductors have the following drawbacks, integrated inductors can be built but

1. Lossy
2. For low frequency, size and weight is very large, can have surface mounted inductors but for higher frequencies
3. Ferromagnetic cores for low frequency inductors, leads to nonlinear inductance
4. Radiation and pickup
5. Quality Factor is proportional to the square of the linear size. Thus, reduced size quickly reduces Q. (by comparison, high Q caps can be built, of the order of 30 to a few hundred integrated, several thousand in discretes.

integrated inductors can be built but can usefully obtain inductors only up to about 10 nH. (100 nH with very specialized techniques, not generally available). Thus these are only useful in the 1 GHz range or above.

- opamps been around since the sixties allowing active filters using resistors and capacitors, starting with integrated opamps, and discrete capacitors and resistors, sometimes chip capacitors and thin film resistors

Fully Integrated

MOS usually chosen because capacitors are good (very low leakage allowing charge storage for a long time, milli seconds to seconds). Typically, leakage < pA, or gate impedance close to infinite.

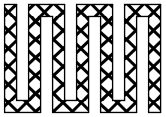
But capacitors take up area. At 500 μm^2 per pF, or about 22 μm per side, a 100 pF capacitor would be quite large, about 220 μm per side.

Common Applications of Integrated Filters

Really anything, but possibly the most common is voice band (telephony) filters in the range of 0-4 kHz. Some reported filters in CMOS up to a few hundred MHz, very experimental. In Bipolar, can build filters at reduced quality up to the GHz frequency range.

Problems with RC Filters

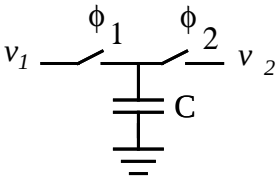
For voice band:

poles ≈ 10 krad/s, $\omega_p = \frac{1}{RC}$, for $C = 10$ pF, $R = 10$ MΩ. If one attempts to use diffusion to build the resistor at about $4\ \text{k}\Omega/\square$ leads to $10^7/4000 = 2500\square$ which might be realized with something 2.5 mm by 1 μm in some snaking configuration as shown below, just to turn the structure into a rectangle or a square. But minimum width can lead to loss of accuracy, so one might instead choose 10 mm by 4 μm. Note a poly resistor which might be more like $30\Omega/\square$, the size is even worse. This would require $10^7/25 = 400000\square$.  In the first example, if the spacing is the same as the width then each 1μm track require 2 μm, then total area is 5000 $(\mu m)^2$ which could be realized as a square with 71 μm on a side. For the 10 mm by 4 μm example, assuming spacing is still 1 μm, then area is 10000 μm x5 μm = 50000 $(\mu m)^2$, or a square with 223 μm on a side.

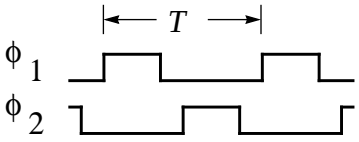
Another problem with such design is that while resistor to resistor matching can be quite good, probably better than 1%, the absolute value is probably no better than 10%. Resistors and capacitors are not correlated in error, thus one could get 20% error in the RC time constant. As well, mismatch could depend on temperature and voltage.

Switched Capacitor as a Resistor

For the following arrangement and the two phase clock as shown:



parallel



timing

Assume when ϕ_1 is high, the switch is closed

-during ϕ_1: $v_c = v_1$, $Q_1 = Cv_1$

-during ϕ_2: $v_c = v_2$, $Q_2 = Cv_2$,

The difference in charge is $\Delta Q = Q_1 - Q_2 = C(v_1 - v_2)$,

for example if $v_1 = 2V$, $v_2 = 1V$, $C = 1F$, $Q_1 = 2$ Coulomb, $Q_2 = 1$ Coulomb

This ΔQ is being "delivered" from v_1 to v_2 every T seconds. Thus over the long term, the rate of charge transfer is on average:

$$\frac{\Delta Q}{t} = i = \frac{C(v_1 - v_2)}{T} = \frac{(v_1 - v_2)}{T/C} = \frac{(v_1 - v_2)}{R_{eq}}$$

Thus, the switched capacitor is performing the same function as a resistor of value $R_{eq} = \frac{T}{C}$.

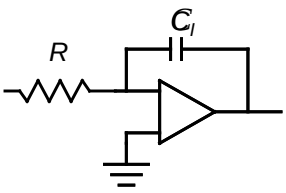
Typical values: $f_c = f_{clock} = 100\text{ kHz} - 100\text{ MHz}$, with no real lower limit, but the upper limit set by settling time, thus $T = 10\text{ ns} - 10\ \mu\text{s}$. $C = 0.1\text{ pF} - 10\text{ pF}$, then $R_{eq} = 10\ \text{k}\Omega - 1\ \text{G}\Omega$.

Let us compare to an actual resistor using resistive material at $30\Omega/\square$, to diffusion at about $4\ \text{k}\Omega/\square$, then:

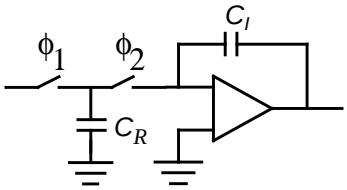
for 1M, need $\frac{10^6}{30} = 33333\square$, or $\frac{100,000\ \mu}{3\ \mu}$ or $\frac{10^6}{4\text{ k}} = 250\square$, or $\frac{750\ \mu}{3\ \mu}$

In comparison, the S.C. uses 1 MHz and 1 pF, where 1 pF takes a square of 22 μm per side.

Switched-Capacitor Integrators



discrete integrator



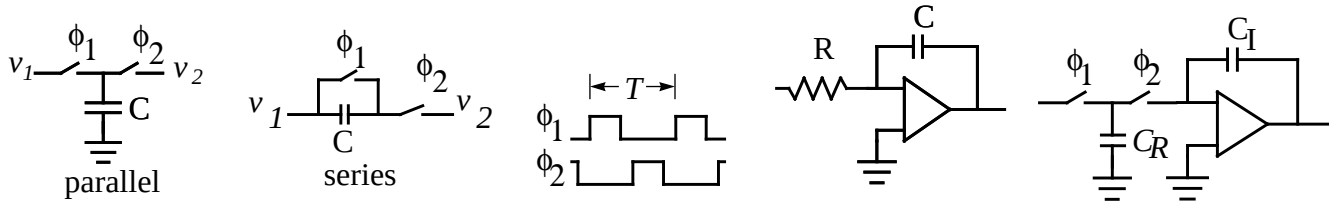
S.C. integrator

$R_{equiv} = \frac{T}{C_R}$, thus for the integrator: $\frac{v_o}{v_i} = -\frac{1}{sC_I R_{equiv}} = -\frac{1}{sT}\frac{C_R}{C_I} = -\frac{\alpha}{sT}$ where $\alpha = \frac{C_R}{C_I}$

For a general filter, the pole frequency is given by $\frac{1}{2\pi RC_1} = f_{pole} = \frac{\alpha}{2\pi T} = \frac{\alpha f_{clock}}{2\pi}$. Thus a pole frequency is defined relative to the clock frequency. Since α is a capacitor ratio, it can be very accurate, e.g., of the order of 0.1%, thus the pole frequency is accurate. T can be derived from a crystal oscillator, thus can be very accurate, leading to very well defined corner frequencies. Comare to RC filter above, since R and C are defined in different processing steps, they do not track. If absolute error is 20% for each, with no correlation, worst case is about 40%, e.g., with R low and C low or R high and C high.

on ϕ_2, $Q_2 = Cv_2$. Thus there has been a net flow of charge between the two voltages sources of have the following: $i = \left(\frac{C}{T}\right)(v_1 - v_2)$. Thus current is linearly related to a voltage difference and hence the circuit is equivalent to a resistor of value $\frac{T}{C}$. These can be combined to form integrators which can be compared to discrete integrators.

The integrator transfer function is $\frac{v_o}{v_i}$.



Switched-Capacitor "Resistors" timing discrete integrator S.C. integrator

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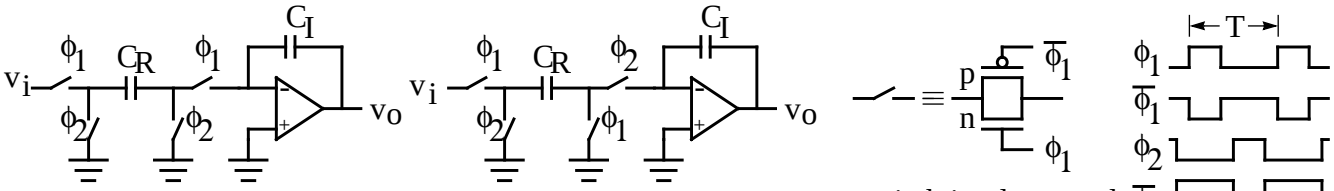


S.C. integrator with stray-free resistor

S.C. integrator with inverting stray-free resistor

switch implemented with pass gate

overall timing

A pass gate is formed by two transistors connected in parallel; an n-channel and a p-channel. In this way the resistance is more uniform over the complete voltage range compared to a single transistor, and allows operation close to the power supply voltages.

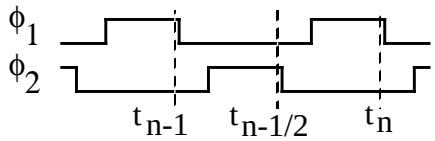
S.C. Analysis using Difference Equations

- **Times are shown at the end of the phase to allow voltages to settle after the transition. Determine the connections for each phase.**

For each transition, the sum of all currents (or charge) into nodes (typically inputs of opamps) is zero. Use the connection at the end of the transition to determine which currents to sum,

- **e.g,. in the $\phi_2 \to \phi_1$ transition (equivalent to $t_{n-1/2} \to t_n$ transition) elements connected to the node during ϕ_1 are considered.**

$$\sum i = \sum \frac{\Delta Q}{T} = \sum \frac{C\Delta V}{T} = 0$$



Where ΔV represents the difference in the voltage across a capacitor before and after the transition, expressed as v_n, $v_{n-1/2}$, etc. Result: Difference equation. For integrators shown above: