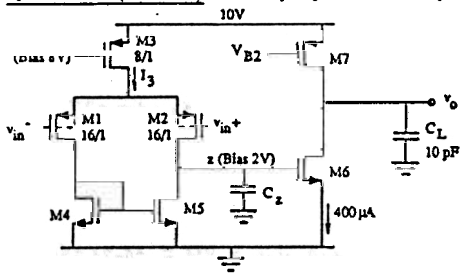
97.477 Analog Integrated Electronics Midterm 3 Nov. 1997 C. Plett

Your Name:

One sheet of notes, 8 1/2 by 11, one side allowed, or official course summary. Do all questions directly on this paper. For extra space or for rough work, use back if necessary. Time 1 hour. - Total Marks 20%.

Question 1. (8 marks) For the opamp as shown and parameters as listed:



$K_{pn} = 100\mu A/V^2$
$K_{pp} = 50\mu A/V^2$
$\lambda_n = 0.02$
$\lambda_p = 0.02$
$V_{Tn} = 1.0V$
$V_{Tp} = -1.0V$

a) Find I_3 $\frac{K_{pp}}{2}\left(\frac{W}{L}\right)_3 V_{on}^2 = 25 \cdot 8 \cdot {}^2 = 200\mu A$

b) What is $(W/L)_5$? $I_5 = 100\mu A = \frac{K_{pn}}{2}\left(\frac{W}{L}\right)_5 V_{on}^2 = 50\left(\frac{W}{L}\right)_5$

$\therefore \left(\frac{W}{L}\right)_5 = 2$

c) What is g_{m1}?

$\sqrt{2K_{pp}\left(\frac{W}{L}\right)_1 I} = \sqrt{2 \cdot 50 \cdot 16 \cdot 100} = 400\mu A/V$

d) What is the resistance seen at the output of the differential stage, i.e., at node z?

$r_{op} = r_{on} = \frac{1}{I\lambda} = \frac{1}{100\mu \cdot 0.02} = 500k\Omega$

$\therefore r_z = 250k\Omega$

e) What is the small-signal low-frequency gain to v_o?

$g_m r_z = 400\mu A/V \times 0.25M\Omega = 100$

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f) Find the negative common-mode input voltage range.

V_{D2} = Goes to 1V

V_z is fixed at 2V. V_{D1} can go to $V_{G2} + |V_T|$

or $|V_{DS2}| \geq |V_{GS2}| - |V_{T2}|$ $\therefore V_{G2} = V_z - |V_T| = 1V$

g) For the output stage, if $(W/L)_6 = (W/L)_7$, what is V_{B2} in volts?

$I = \frac{K_p}{2}\frac{W}{L}V_{on}^2$ if $\frac{W}{L}$ is same, $K_{pp} = \frac{1}{2}K_{pn}$

$\therefore V_{onp} = \sqrt{2}\,V_{onn} = 1.414V$, $V_{GS} = 2.414$

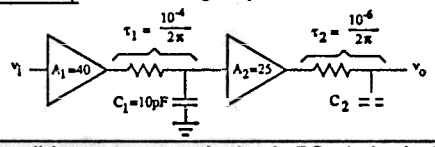
$\therefore V_{B2} = 10 - 2.414 = 7.586V$

h) If the voltage on node z is stepped to 1 V, what is the slew rate in C_L?

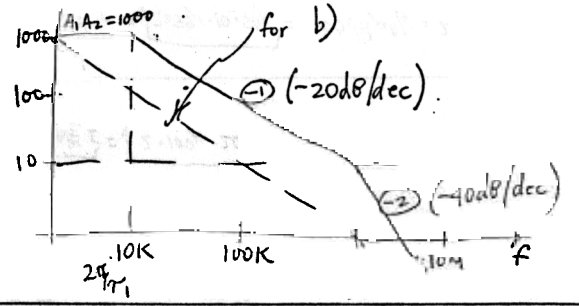
M6 turns off $I_C = 400\mu A$

$S.R. = \frac{I}{C} = \frac{400\mu A}{10pF} = 40V/\mu s.$

Question 2. (4 marks) For the two stage amplifier shown:



a) Sketch the overall frequency response showing the DC gain, breakpoints and slopes.



b) To what value should C_1 be changed to provide about 45° of phase margin?

Need C_1 10 times bigger to move f_{p1} to 1KHz

$C = 100pF$

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Question 3. (3 marks) An opamp has its frequency response dominated by a single low-frequency pole. It has DC gain of 10^4 (80 dB) and unity-gain bandwidth of 10 MHz.

a) Assume this amplifier is used in closed loop to design a bandpass filter which has resonant frequency of 10 kHz and an ideal closed-loop gain at the resonant frequency = 10 (i.e., 20 dB). What is the gain error and the corrected gain at the resonance frequency?

At 10 kHz

$A = 1000$ or 60dB

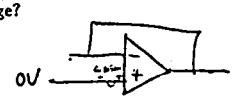
$B = \frac{1}{10}$ or $\frac{1}{B} = 10$ or 20dB

$A_{CL} = \frac{A}{AB} = 100$

Gain error $= \frac{1}{100}$

gain $\approx$ 9.9

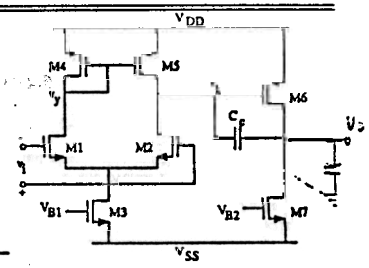
b) Now assume this opamp has an offset referred to the output of 0.5 V. If the opamp is connected as a unity gain buffer and 0 V is applied at the input, what will be the output voltage?



$V_{i,eff} = \frac{0.5V}{10^4} = 0.05mV$

$\therefore V_o = 0.05\ mV$

Question 4. (5 Marks) In a CMOS opamp such as designed in the lab; if for each transistor, both W and L are doubled, but all the bias levels (V_{DD}, V_{SS}, V_{B1}, V_{B2}, V_{IN} remain the same:



a) what will happen to the current?

current remains the same $\frac{W}{L}$ is same

b) what will happen to the DC gain?

$r_o \propto \frac{1}{I\lambda}$ $\lambda \propto \frac{1}{L}$ $\therefore$ r_o about twice

each stage gain is twice, overall 4 times

c) what will happen to the common-mode rejection ratio?

$CMRR = \frac{A_D}{A_C} =$ up 4 times $\frac{g_{m1} r_z g_{m6} r_o}{\times Y_2 \rightarrow \frac{1}{2}\frac{g_{m3}}{g_{m1}} \cdot g_{m6} r_o}$

up 4 times