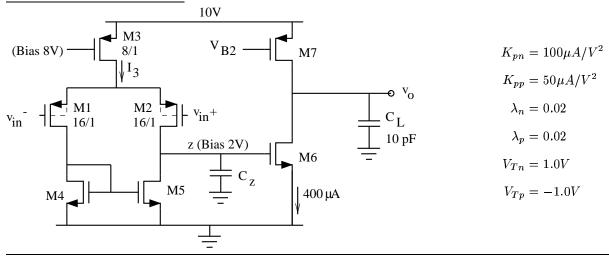
97.477 Analog Integrated Electronics Midterm 3 Nov. 1997 C. Plett

Your Name:

One sheet of notes, $8\ 1/2$ by 11, one side allowed, or official course summary. Do all questions directly on this paper. For extra space or for rough work, use back if necessary. Time 1 hour. - Total Marks 20%.

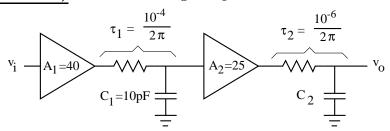
Question 1. (8 marks) For the opamp as shown and parameters as listed:



- a) Find I_3
- b) What is $(W/L)_5$?
- c) What is g_{m1} ?
- d) What is the resistance seen at the output of the differential stage, i.e., at node z?
- e) What is the small-signal low-frequency gain to v_z ?

- f) Find the negative common-mode input voltage range.
- g) For the output stage, if $(W/L)_6 = (W/L)_7$, what is V_{B2} in volts?
- h) If the voltage on node z is stepped to 1 V, what is the slew rate in C_L ?

Question 2. (4 marks) For the two stage amplifier shown:



a) Sketch the overall frequency response showing the DC gain, breakpoints and slopes.

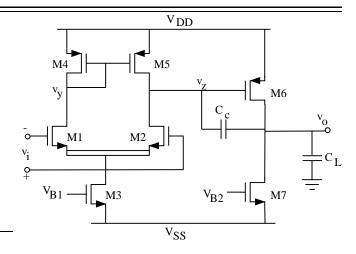
b) To what value should C_1 be changed to provide about 45° of phase margin?

Question 3. (3 marks) An opamp has its frequency response dominated by a single low-frequency pole. It has DC gain of 10⁴ (80 dB) and unity-gain bandwidth of 10 MHz.

a) Assume this amplifier is used in closed loop to design a bandpass filter which has a resonant frequency of 10 kHz and an ideal closed-loop gain at the resonant frequency = 10 (i.e., 20 dB). What is the gain error and the corrected gain at the resonant frequency?

b) Now assume this opamp has an offset referred to the output of 0.5 V. If the opamp is connected as a unity gain buffer and 0 V is applied at the input, what will be the output voltage?

Question 4. (5 Marks) In a CMOS opamp such as designed in the lab; if for each transistor, both W and L are doubled, but all the bias levels $(V_{DD}, V_{SS}, V_{B1}, V_{B2}, V_{IN})$ remain the same:



- a) what will happen to the current?
- b) what will happen to the DC gain?
- c) what will happen to the common-mode rejection ratio?