97.477 lab 4 Switched-Capacitor Filter March 17, 1999

Design a switched-capacitor lowpass biquad filter as described in the following lab information. The clock frequency should be about 32 kHz. The pole frequency is 1 kHz and the DC gain is 20 dB. Design for both a Q of 1 and a Q of 10.

1) By driving the filter with a variable frequency sine wave, and observing with an oscilloscope:

   a) Explore the frequency response from DC to $2F_{clock}$.

   b) Observe, understand and explain the effects of:

      i) Replication

      ii) Aliasing

      ii) Sinx/x

   Note: spectrum analyzers are also available in the lab.

2) By driving the filter with a low-frequency square wave, obtain the transient response for the Q=1 and the Q=10 case. Record the relevant information for the Q=1 case to be used later to compare to theory (shown in Figure 2b for RC biquad with Q=1).

More Details for Integrated Circuit Active Filters

In this lab, a lab version of a switched-capacitor filter will be studied which will show how active filters are being integrated in MOS LSI technology for communications application. The context would be, for example, to integrate a lowpass anti-alias filter as required to bandlimit the input signal below half the sampling frequency. Another example would be an integrated notch filter, which removes 60 Hz noise from the input signal before it gets into the rest of the system. Another example would be a high-Q bandpass filter, used for tuning purposes in a touch-tone telephone tone detector.

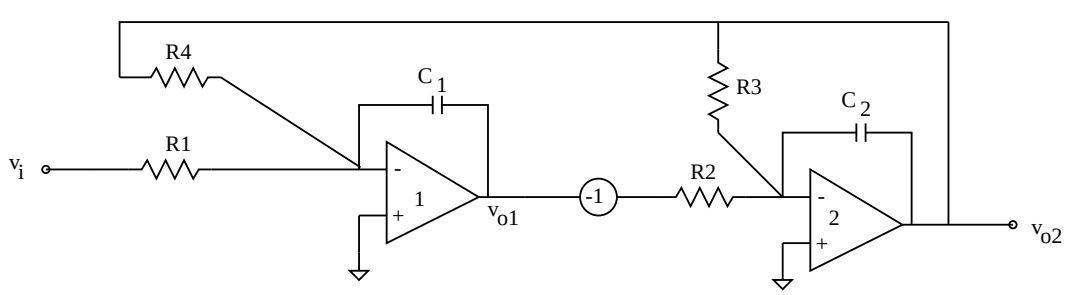

Figure 1 Biquad Filter with Resistors and Capacitors

Consider the active circuit shown in Figure 1, (a "biquad"). The transfer function between V_{in} and V_{o2} can be shown to be:

$$\frac{V_{o2}}{V_{in}} = -\frac{\frac{1}{R_1C_1R_2C_2}}{s^2 + s\frac{1}{R_3C_2} + \frac{1}{R_4C_1R_2C_2}} = -\frac{A_0\omega_p^2}{s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2} \tag{1}$$

This represents a lowpass filter with a DC gain A_0 and pole frequency ω_p given by:

$$A_0 = -\frac{R_4}{R_1} \tag{2}$$

$$\omega_p = \frac{1}{\sqrt{R_4C_1R_2C_2}} \tag{3}$$

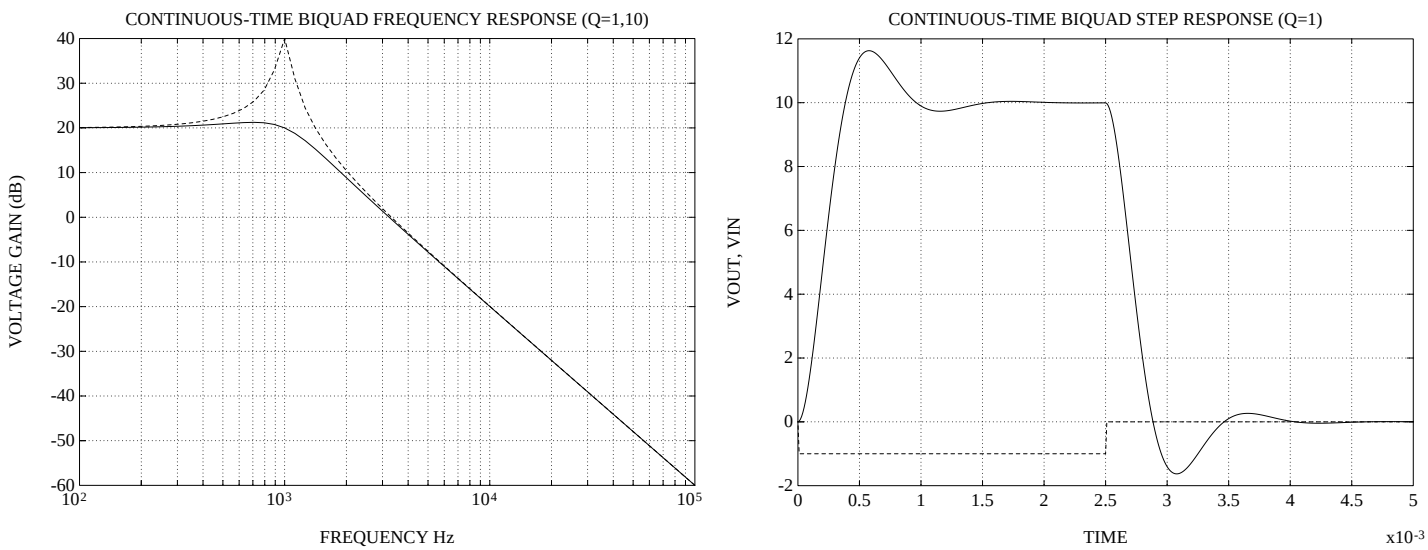

Figure 2 Second-Order Filter a) Frequency Response and b) Time Response to -1V Step

In an integrated MOS LSI circuit, such filters are being realized nowadays using "switched-capacitor resistors", which imitate the action of the resistors in a sampled data circuit with capacitors and switches - as shown in Figure 3.

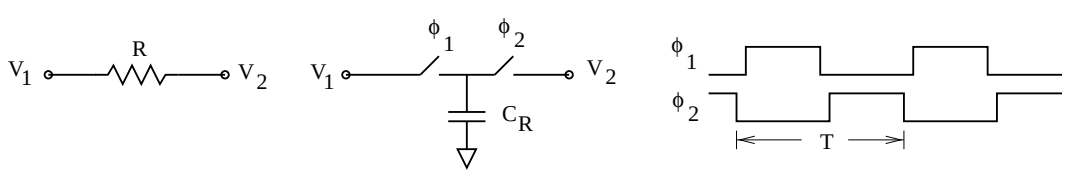

Figure 3 Switched Capacitor Equivalent to Resistor

with the result that the equivalent resistor value is equal to:

$$R = \frac{T}{C_R} \tag{4}$$

Here ϕ_1 and ϕ_2 are non-overlapping two-phase clocks. The action is to charge C_R alternately to V_1 and V_2 so as to pass the same amount of charge between the nodes V_1 and V_2, in one clock period T, as the continuous resistor R would have passed.

In practice, more complicated switching than the above is used, to make the circuit insensitive to stray capacitances. Figure 4 shows a typical switching arrangement that gives a circuit which more or less duplicates the filter behaviour of the Figure 1 circuit.

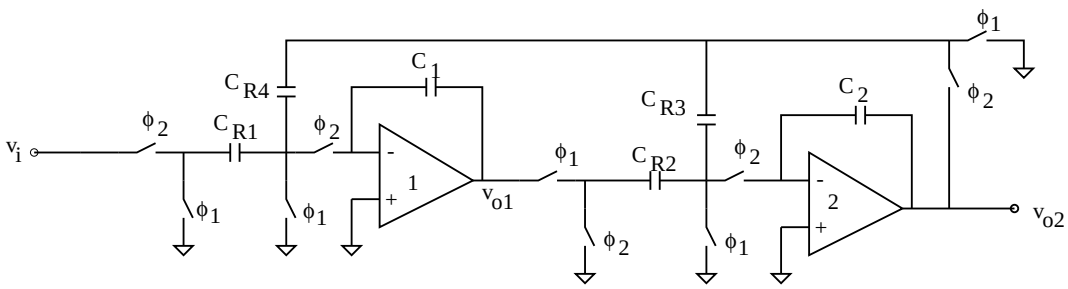

Figure 4 Switched-Capacitor Biquad Filter

Note that ϕ_1 and ϕ_2 cannot be overlapping, although their rise and falls can be very close together, Also note that the inversion required in Figure 1 (gain of -1) is accomplished by arranging the switches around C_{R2} to invert it after it samples the signal from opamp 1.

<u>Design Procedure</u> (to achieve a filter with specifications as in Figure 2.)

i) Choose $C_1 = C_2 = 1000$ pF (fixed on the board).

ii) Choose $R_1 = R_2 = R$ and use Eqn. 3 to get the value of R.

iii) From Eqn. 4, get the required C_R, assuming sampling frequency of 32 kHz.

iv) From the desired DC gain of 20 dB, get the size of R_1.

v) The value of Q_p can be solved from Eqn. 1, where

$$\frac{\omega_p}{Q_p} = \frac{1}{R_3 C_2} \qquad \text{or} \qquad Q = \frac{R_3}{R} \tag{5}$$

$Q_P \approx 1$ is chosen to result in the sharpest corner around ω_p without too much overshoot. Also try a high value, $Q_p = 10$ to see the effects of the overshoot.

Thus from the desired value of R_3 obtained from Eqn. 5, find the value for C_{R3} in Figure 4. For example, for $Q = 10$, $R_3/R = 10$ and therefore $C_{R3} = 0.1C_R$.

<u>Breadboard Filter</u>

The circuit of Figure 4 is available on a printed circuit board. The TL084 opamps

have JFET inputs providing a high input impedance. Analog transmission gates are 4016 (or 4066) CMOS quad analog switches. The required design is to determine the appropriate sizes for C_{R1}, C_{R2}, C_{R3}, C_{R4} and for the capacitor which determines clock frequency.

The clock generator (Figure 5) consists of a ring connection of 3 inverters. The frequency f_{MC} is set by the resistor and capacitor values (R and C) and by the gate delays as given approximately by the following equation:

$$f_{MC} = \frac{1}{0.2\mu\text{sec} + 2.2RC} \tag{6}$$

The resultant analog switch control pulses, ϕ_1 and ϕ_2 should be used to sample at a rate of 32 kHz. This will require a master clock frequency of 1.024 MHz. To eliminate any errors caused by both switches being closed at one time, 25% duty cycle, non-overlapping pulses have been generated through the use of a Johnson counter.

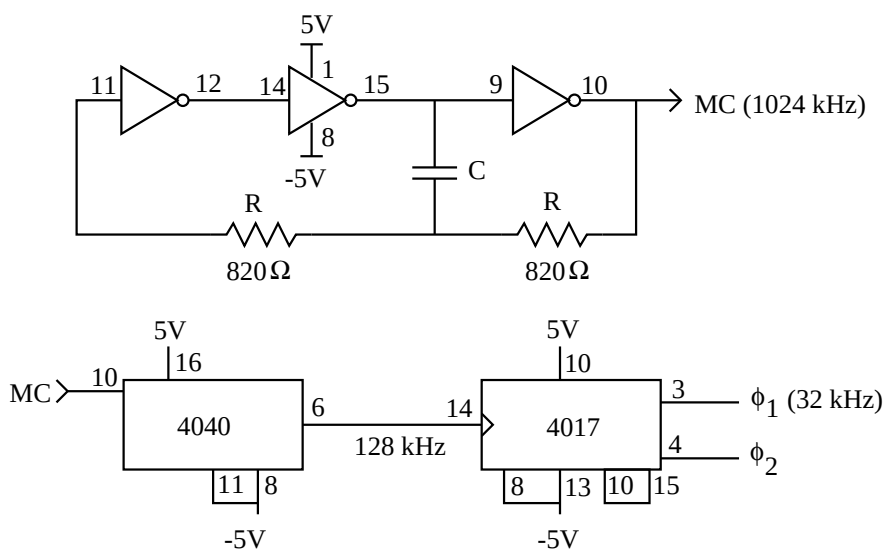

Figure 5 Clock Generator Circuit.