Marking Scheme

Don't use extra words (you don't have to put introduction and background theory)

1. Give the theoretical design procedures of how you design the opamp to achieve the specification. For example, slew rate calculation, W/L calculations, choice of biasing etc. List the W/L of all transistors, and the bias voltages. Include a page of transistor internal parameters (gm, go, Id, Cgs etc) from the spice output. Don't submit the input netlist or the whole spice output.

2 - choosing the current source

20 - W/L of all transistors and its bias, if necessary [2 for each transistor]

13 2. Plot the graphs to show that the specifications are met. Clearly label the curves with the following figure of merits: DC operating point [1], dynamic range [1], DC gain[1], UGBW [1], phase margin [1], CM gain [1], slew rates[1], and settling times [4] for both open and close loops. What does phase margin tell you about the opamp? [2]

27 3. Compare the following figure of merits between the theoretical and simulated values: maximum input and output range for differential mode and common mode [5], DC gain [5], UGBW [5], phase margin [5], slew rate[2], and the close loop gain [5].

5 4. According to Fig. 2 (closed-loop), what is the equivalent output load? Why is 2pF used as the load in the open-loop simulation[2]? If the load were doubled to 4pF, how would this affect DC gain [1], UGBW [1], and the slew rates[1]?

8 5. Compare the simulated DC gain and UGBW between the differential pair as in lab 2 and the folded-cascode circuit as in Lab 3. Explain which of the transistors are causing the enhancement, and by how much? Explain and calculate the improvement using the theoretical small-signal model [6]. Compare the simulated and the theoretical improvement [2].

5 6. Calculate CMRR [2]. Which transistor (labelled as in Fig. 1) has the greatest impact to this figure of merit [1]? What happens if the common gain is too large? How would this degrade the circuit performance [2]?

5 7. Summarize your report with a table of your folded-cascode opamp specifications: given load, DC gain, UGBW, phase margin, slew rate, CMRR, and power consumption.

85% Report + 15% Lab = 100%

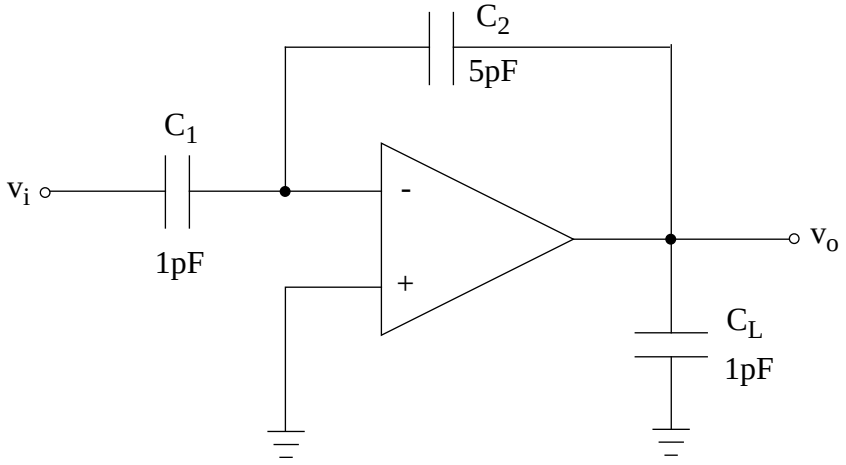

Figure 2 Closed-Loop Opamp

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* Lab3: folded cascode opamp
M1 5 1 3  0  MNCH_0P8 L=0.8U W=10.0U M=1
M2 6 2 3  0  MNCH_0P8 L=0.8U W=10.0U M=1
* current source
I3   3 0 180U
R3   3 0 22K
* current source load
M4   5  7 99 99 MPCH_0P8 L=0.8U W=10.0U M=1
M5   6  7 99 99 MPCH_0P8 L=0.8U W=10.0U M=1
M6   8 10  5 99 MPCH_2P0 L=2.0U W=10.0U M=1
M7   9 10  6 99 MPCH_2P0 L=2.0U W=10.0U M=1
M8   8 11 12  0 MNCH_2P0 L=2.0U W=10.0U
          M=1
M9   9 11 13  0 MNCH_2P0 L=2.0U W=10.0U
          M=1
M10 12 14  0  0 MNCH_2P0 L=2.0U W=10.0U
          M=1
M11 13 14  0  0 MNCH_2P0 L=2.0U W=10.0U
          M=1
*
* capacitive load
CL   8  0  2E-12
* DC voltage bias
VDD 99  0  DC 3.0V
VB1  7  0  DC 1V
VB2 10  0  DC 1V
VB3 11  0  DC 1V
* analog ground
Vag 98 0 DC 1.5
* voltage control voltage source for differential
          input
Ei 2 98 1 98 -1
* input for DC and AC analysis
Vi 1 98 DC 0 AC 0.5
* TR anaylsis (V_initial V_final delay rise_time
          fall_time pulse_width period)
* Vi 1 98 PULSE ( -1.5V 1.5V 1US 10PS 10PS
          1US 20US )
* DC, AC and transient analysis
* DC: node V_start V_stop V_step
* AC: mode number_of_freq_points_per_decade
          freq_start freq_stop
*     (mode: LIN=linear sweep DEC=log sweep)
* TR: Time_delay Time_stop
.DC Vi -1 1 1E-3
*.AC DEC 10 10 1E9
*.TRAN 0.25US 4US
.PROBE
.OP
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Figure 3 Folded-Cascode Opamp Spice Deck

97.477 Lab 3 Folded-Cascode Opamp

Modify the differential opamp designed in Lab 2 to a folded-cascode opamp (Fig. 1) with the following specifications as given in Lab2:

a) the nominal DC operating points for both inputs v_i and output v_o are 1.5V with a 3V V_{DD} supply, and the load capacitance is again 2pF;

b) DC gain has to be greater 40dB, with the phase margin greater than 50 degrees;

c) the slew rate has to be greater than 100V/µs.

You are free to adjust other DC biases. The suggested V_{on} is 0.2 to 0.3V. After the specifications are met, close the loop as shown in Fig. 2. Apply a 3V step at the input. Determine the closed-loop opamp gain and the 99% settling time. A report is required for this lab.

For initial sizing, you may assume that $K_{pn} = 75\ \mu A/V^2$, $K_{pp} = 25\ \mu A/V^2$, $\lambda_n = \lambda_p = 0.2$ for $L = 2\ \mu m$. These numbers are not very accurate (e.g., λ_n is good but λ_p is a bit lower) but should get you into the right range. Note that M3 has been replaced by an equivalent current source and resistor, because some simulators cannot handle more than 10 transistors.

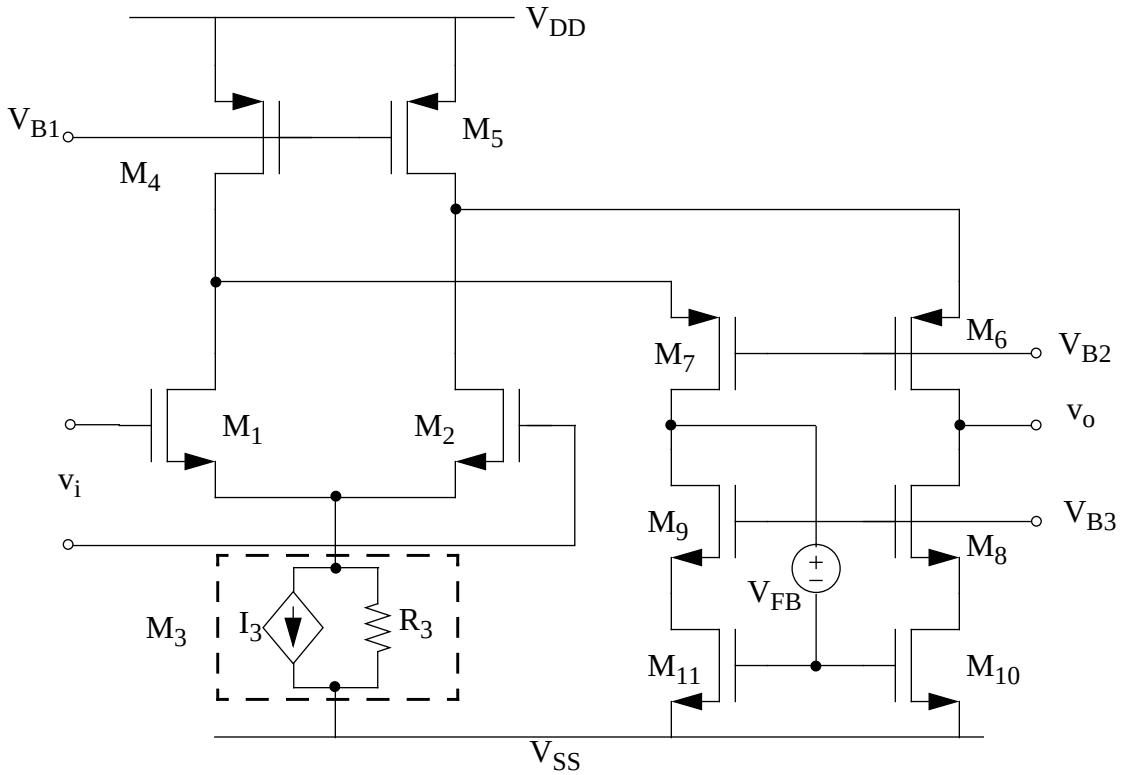

Figure 1 A Folded-Cascode Opamp