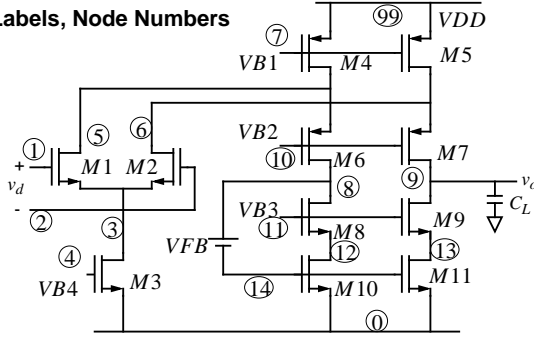


NMOS Input, Single-Ended Output, Folded-Cascode Amplifier Example (node 8 fed back to node 14)

Labels, Node Numbers



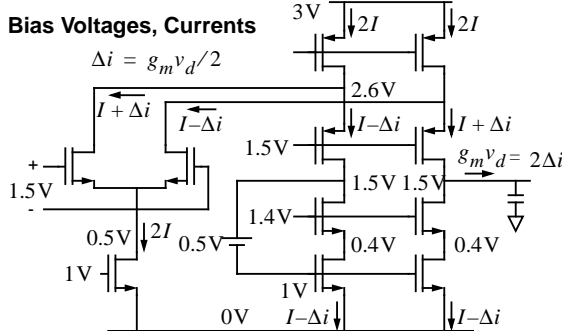
If v_{on} is picked to be 0.2 V, and $V_{TN} = 0.8V$,
 $V_{TP} = -0.9V$, then $V_{GSN} = 1.0V$, $|V_{GSP}| = 1.1V$.

Minimum possible V_{DS} is v_{on} , however, to be safe, set to $v_{on} + 0.2V = 0.4V$, power supply rails at 3.0 V. (bias voltages shown below) then swing from about 0.6 V to 2.4 V.

Initial estimates: $K_{pn} = 75 \mu A/V$, $K_{pp} = 25 \mu A/V$,
 $\lambda_{n,p} = 0.2$ for $L = 2 \mu m$, $\lambda_{n,p} = 0.5$ for $L = 0.8 \mu m$

$$I_{DS} = \frac{K_p W}{2L} v_{on}^2 (1 + \lambda V_{DS}), g_o = I_{DS} \lambda, r_o = 1/(I_{DS} \lambda)$$

Bias Voltages, Currents



* Initial Values calculated as above

M1	5	1	3	0	MNCH_0P8	L=0.8U	W=26.0U	M=1
M2	6	2	3	0	MNCH_0P8	L=0.8U	W=26.0U	M=1
M3	3	4	0	0	MNCH_2P0	L=2.0U	W=242.U	M=1
M4	5	7	99	99	MPCH_0P8	L=0.8U	W=267.U	M=1
M5	6	7	99	99	MPCH_0P8	L=0.8U	W=267.U	M=1
M6	8	10	5	5	MPCH_2P0	L=2.0U	W=326.U	M=1
M7	9	10	6	6	MPCH_2P0	L=2.0U	W=326.U	M=1
M8	8	11	12	0	MNCH_2P0	L=2.0U	W=110U	M=1
M9	9	11	13	0	MNCH_2P0	L=2.0U	W=110U	M=1
M10	12	14	0	0	MNCH_2P0	L=2.0U	W=110U	M=1
M11	13	14	0	0	MNCH_2P0	L=2.0U	W=110U	M=1

Note, M3 is replaced by current source of 180 μA and 25 k Ω resistor which provides 20 μA at 0.5 V. Results shown on next page. Biggest problem: current through M4, M5 is way too big. Fix this first before adjusting more minor problems. E.g., v_{on} not at 0.4 V, v_o not exactly at 1.5 V.

Folded-Cascode Opamp Design Example: C. Plett

Results of initial simulations with sizes on previous page, M3 current source

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	1.5000	(2)	1.5000	(3)	.5256	(5)	2.7406
(6)	2.7406	(7)	1.9000	(8)	1.6425	(9)	1.6425
(10)	1.5000	(11)	1.4000	(12)	.2341	(13)	.2341
(14)	1.1425	(98)	1.5000	(99)	3.0000		

NAME	M1	M2	M4	M5	M6	M7	M8	M9	M10	M11
MODEL	MNCH_0P8	MPCH_0P8	MPCH_0P8	MPCH_0P8	MPCH_2P0	MPCH_2P0	MNCH_2P0	MNCH_2P0	MNCH_2P0	MNCH_2P0
ID	1.01E-04	1.01E-04	-3.78E-04	-3.78E-04	-2.77E-04	-2.77E-04	2.77E-04	2.77E-04	2.77E-04	2.77E-04
VGS	9.74E-01	9.74E-01	-1.10E+00	-1.10E+00	-1.24E+00	-1.24E+00	1.17E+00	1.17E+00	1.14E+00	1.14E+00
VDS	2.22E+00	2.22E+00	-2.59E-01	-2.59E-01	-1.10E+00	-1.10E+00	1.41E+00	1.41E+00	2.34E-01	2.34E-01
VBS	-5.26E-01	-5.26E-01	0.00E+00	0.00E+00	0.00E+00	0.00E+00	-2.34E-01	-2.34E-01	0.00E+00	0.00E+00
VTH	7.61E-01	7.61E-01	-8.50E-01	-8.50E-01	-9.22E-01	-9.22E-01	8.68E-01	8.68E-01	8.33E-01	8.33E-01
VDSAT	2.22E-01	2.22E-01	-2.63E-01	-2.63E-01	-3.20E-01	-3.20E-01	2.99E-01	2.99E-01	3.05E-01	3.05E-01
GM	7.32E-04	7.32E-04	2.43E-03	2.43E-03	1.47E-03	1.47E-03	1.56E-03	1.56E-03	1.22E-03	1.22E-03
GDS	3.91E-05	3.91E-05	2.15E-04	2.15E-04	2.00E-05	2.00E-05	3.72E-05	3.72E-05	4.64E-04	4.64E-04
GMB	1.17E-04	1.17E-04	4.64E-04	4.64E-04	4.02E-04	4.02E-04	3.85E-04	3.85E-04	3.49E-04	3.49E-04
CGSOV	7.47E-15	7.47E-15	5.73E-14	5.73E-14	7.00E-14	7.00E-14	3.17E-14	3.17E-14	3.17E-14	3.17E-14
CGDOV	7.47E-15	7.47E-15	5.73E-14	5.73E-14	7.00E-14	7.00E-14	3.17E-14	3.17E-14	3.17E-14	3.17E-14
CGBOV	3.72E-16	3.72E-16	4.54E-16	4.54E-16	1.14E-15	1.14E-15	1.05E-15	1.05E-15	1.05E-15	1.05E-15
CGS	2.23E-14	2.23E-14	2.80E-13	2.80E-13	8.55E-13	8.55E-13	2.68E-13	2.68E-13	2.25E-13	2.25E-13
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	1.27E-13	1.27E-13

Notes: CBD, CBS, CGB left out as they are all zeros. M6 and M7 has VSB=0, (no body effect) allows VGS also of 1.1 V, (this option is not available with M8, M9, or M1, M2). Current in M4, M5 is very high, attempt to scale W by 200/378, result (W/L) of about 140. Also, VGS of M1 and M2 is a bit low, could make these transistors a bit smaller. After that, first adjust I4, I5 to 200 μA , before any adjustments can be done on M6, through M10. Next page shows results after M4, M5 adjusted to give 200 μA , and M1, M2 adjusted slightly to have VGS of 1V. Note, on next page, all capacitance parameters left out of table.

Folded-Cascode Opamp Design Example: C. Plett

M4, M5 adjusted to give about 200 uA, and M1, M2 adjusted slightly to have VGS of 1V

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	1.5000	(2)	1.5000	(3)	.4991	(5)	2.5919
(6)	2.5919	(7)	1.9000	(8)	1.4893	(9)	1.4893
(10)	1.5000	(11)	1.4000	(12)	.3415	(13)	.3415
(14)	.9893	(98)	1.5000	(99)	3.0000		

NAME	M1	M2	M4	M5	M6	M7	M8	M9	M10	M11
MODEL	MNCH_0P8	MNCH_0P8	MPCH_0P8	MPCH_0P8	MPCH_2P0	MPCH_2P0	MNCH_2P0	MNCH_2P0	MNCH_2P0	MNCH_2P0
ID	1.00E-04	1.00E-04	-2.01E-04	-2.01E-04	-1.01E-04	-1.01E-04	1.01E-04	1.01E-04	1.01E-04	1.01E-04
VGS	1.00E+00	1.00E+00	-1.10E+00	-1.10E+00	-1.09E+00	-1.09E+00	1.06E+00	1.06E+00	9.89E-01	9.89E-01
VDS	2.09E+00	2.09E+00	-4.08E-01	-4.08E-01	-1.10E+00	-1.10E+00	1.15E+00	1.15E+00	3.41E-01	3.41E-01
VBS	-4.99E-01	-4.99E-01	0.00E+00	0.00E+00	0.00E+00	0.00E+00	-3.41E-01	-3.41E-01	0.00E+00	0.00E+00
VTH	7.64E-01	7.64E-01	-8.40E-01	-8.40E-01	-9.21E-01	-9.21E-01	9.00E-01	9.00E-01	8.30E-01	8.30E-01
VDSAT	2.41E-01	2.41E-01	-2.71E-01	-2.71E-01	-1.91E-01	-1.91E-01	1.81E-01	1.81E-01	1.79E-01	1.79E-01
GM	6.64E-04	6.64E-04	1.27E-03	1.27E-03	9.06E-04	9.06E-04	9.63E-04	9.63E-04	9.53E-04	9.53E-04
GDS	3.55E-05	3.55E-05	8.40E-05	8.40E-05	1.22E-05	1.22E-05	2.30E-05	2.30E-05	2.27E-05	2.27E-05

- Notes: M1, M2, have the expected voltage.
- M4, and M5 have the correct current, and the voltage is nearly as expected (expected VDS to be 0.4 V, it is 0.408. Thus VGS of M6 and M7 are a bit too small, could decrease the size of M6, M7 a bit.
 - How much? To get $V_{GS} = 1.1 \text{ V}$, requires a $\Delta V = 0.01 \text{ V}$. This will change the current by $g_m \times 0.01 = 9.06 \mu\text{A}$. Present current is correct at $101 \mu\text{A}$, To reduce by $9.06 \mu\text{A}$ requires change of size by $92/100$ times.
- M10, M11 set the output voltage, since $V_{GS10} + V_{FB} = V_O$. Output voltage is a bit low, need larger VGS across M10, M11 so decrease their size a bit. Similar to case for M6, M7: need $\Delta V = 0.011$, will increase current by $g_m \times 0.011$ about $10 \mu\text{A}$, then compensate by decreasing W by about $91/101$.
- M8, M9 set the voltage on node 12, 13 since it is voltage on node 11 minus VGS. Since VDS of M10 is only 0.34, need smaller VGS of M8, M9. Could try larger W/L, however, VT is increased because of body effect, so VGS of 1V may be hard to achieve. Instead could increase VB3 slightly (here to 1.48V).

Folded-Cascode Opamp Design Example: C. Plett

Simulations after all currents adjusted, VGS of NMOS all 1V, PMOS 1.1V, VDS set to 0.4V (used VB3=1.48V)

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	1.5000	(2)	1.5000	(3)	.4995	(5)	2.6005
(6)	2.6005	(7)	1.9000	(8)	1.4976	(9)	1.4976
(10)	1.5000	(11)	1.4800	(12)	.3977	(13)	.3977
(14)	.9976	(98)	1.5000	(99)	3.0000		

NAME	M1	M2	M4	M5	M6	M7	M8	M9	M10	M11
MODEL	MNCH_0P8	MNCH_0P8	MPCH_0P8	MPCH_0P8	MPCH_2P0	MPCH_2P0	MNCH_2P0	MNCH_2P0	MNCH_2P0	MNCH_2P0
ID	1.00E-04	1.00E-04	-2.00E-04	-2.00E-04	-1.00E-04	-1.00E-04	1.00E-04	1.00E-04	1.00E-04	1.00E-04
VGS	1.00E+00	1.00E+00	-1.10E+00	-1.10E+00	-1.10E+00	-1.10E+00	1.08E+00	1.08E+00	9.98E-01	9.98E-01
VDS	2.10E+00	2.10E+00	-3.99E-01	-3.99E-01	-1.10E+00	-1.10E+00	1.10E+00	1.10E+00	3.98E-01	3.98E-01
VBS	-5.00E-01	-5.00E-01	0.00E+00	0.00E+00	0.00E+00	0.00E+00	-3.98E-01	-3.98E-01	0.00E+00	0.00E+00
VTH	7.64E-01	7.64E-01	-8.41E-01	-8.41E-01	-9.21E-01	-9.21E-01	9.15E-01	9.15E-01	8.29E-01	8.29E-01
VDSAT	2.41E-01	2.41E-01	-2.71E-01	-2.71E-01	-1.99E-01	-1.99E-01	1.89E-01	1.89E-01	1.87E-01	1.87E-01
GM	6.64E-04	6.64E-04	1.27E-03	1.27E-03	8.65E-04	8.65E-04	9.15E-04	9.15E-04	9.03E-04	9.03E-04
GDS	3.55E-05	3.55E-05	8.39E-05	8.39E-05	1.17E-05	1.17E-05	2.18E-05	2.18E-05	2.16E-05	2.16E-05
GMB	1.08E-04	1.08E-04	2.42E-04	2.42E-04	2.40E-04	2.40E-04	2.12E-04	2.12E-04	2.59E-04	2.59E-04
CGSOV	6.32E-15	6.32E-15	2.85E-14	2.85E-14	6.44E-14	6.44E-14	2.88E-14	2.88E-14	2.88E-14	2.88E-14
CGDOV	6.32E-15	6.32E-15	2.85E-14	2.85E-14	6.44E-14	6.44E-14	2.88E-14	2.88E-14	2.88E-14	2.88E-14
CGBOV	3.72E-16	3.72E-16	4.54E-16	4.54E-16	1.14E-15	1.14E-15	1.05E-15	1.05E-15	1.05E-15	1.05E-15
CGS	1.88E-14	1.88E-14	1.39E-13	1.39E-13	7.87E-13	7.87E-13	2.43E-13	2.43E-13	2.43E-13	2.43E-13

Results and further refinements showing effect of 0.8 micron for M6, M7 and effect of larger W/L for M1, M2.

L of	W/L of	DC Gain	UGBW	Phs Marg	$g_{m1,2}$	$g_{o1,2}$	$g_{m6,7}$	$g_{o6,7}$	Comments
M6,M7	M1,M2	dB	MHz	Degrees	$\mu\text{A/V}$	$\mu\text{A/V}$	$\mu\text{A/V}$	$\mu\text{A/V}$	
2 μ	22/0.8	50.2	42	70	664	35.5	865	11.7	Design as above, cascode L=2 micron for M6, M7,
0.8 μ	22/0.8	39.6	44.6	82	664	35.5	685	45.2	Cascode L=0.8 micron, reduced gain, less phase shift
0.8 μ	44/0.8	41.9	63.5	77.5	979	52.3	683	45.1	Previous design, increase W/L of M1, M2, higher UGBW
0.8 μ	88/0.8	43.8	88.2	72.0	1420	75.9	683	45.1	Increase of W/L of M1, M2, higer UGBW, poorer phase
0.8 μ	176/0.8	45.4	118	65.0	2050	109	684	45.2	Increase W/L of M1, M2, higer UGBW, poorer phase
0.8 μ	352/0.8	46.7	153	55.0	2940	157	684	45.2	Increase W/L of M1, M2, higer UGBW, phase margin limit

Folded-Cascode Opamp Design Example: C. Plett