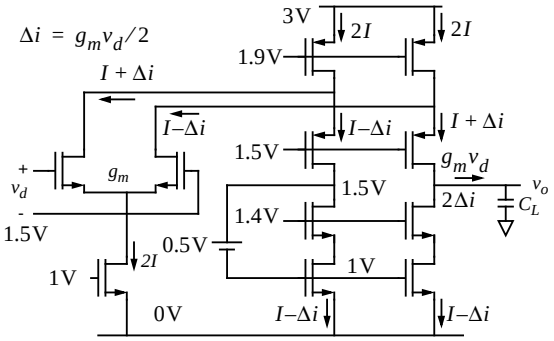
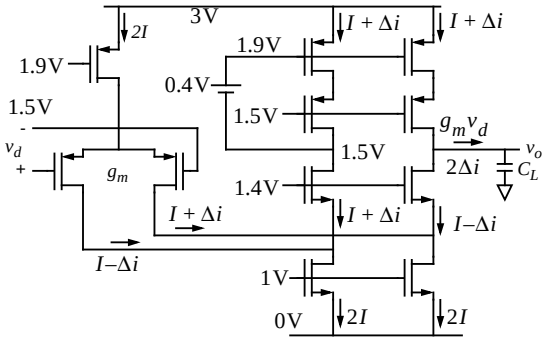
- **Example: If v_{on} is picked to be 0.2 V, V_{DS} set to $V_{on} + 0.2\text{V} = 0.4\text{V}$, $V_{TN} = 0.8\text{V}$, $V_{TP} = -0.9\text{V}$, power supply rails at 3.0 V, (bias voltages shown below) then swing from about 0.6 V to 2.4 V.**



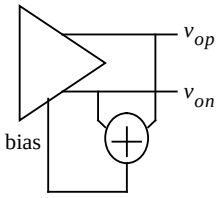


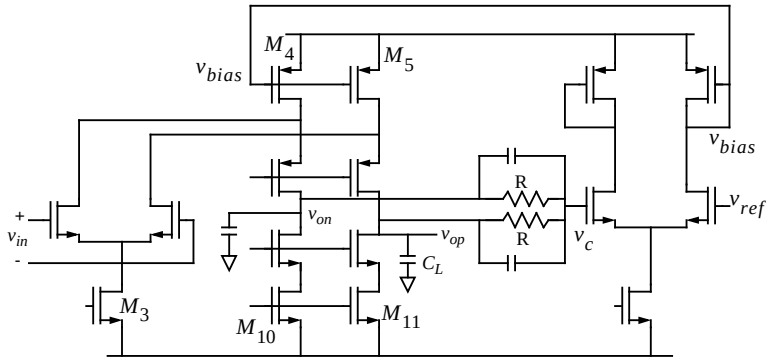
Common-Mode Feedback Circuits

- **single stage (output current is directly $g_m v_d$) high frequency capability**
- **gain = $\frac{v_o}{v_d} = g_m R_o$, typical gain about 1000 or 60 dB. R_o is high due to cascodes**
- **Dominant pole, UGBW is set by load capacitance thus larger load results in more stability**
- **Set current by desired slew rate and known capacitor load.**

- **Circuit and feedback often define difference mode**
- **Common mode can drift, potentially putting circuit into bad region of operation**
- **Need common-mode correction circuit to provide low A_c, with minimal reduction of A_d**
- **Can sum outputs to obtain v_{oc}. If this is not zero, feed back a correcting signal. If output is purely differential, $v_{op} = -v_{on}$ and the sum will be zero. An example below uses resistors for summing**

Example of Common-Mode Feedback Circuit for Folded-Cascode Amplifier

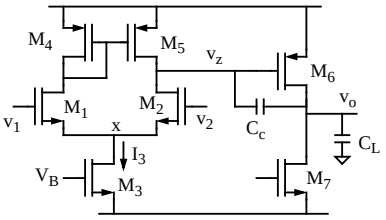


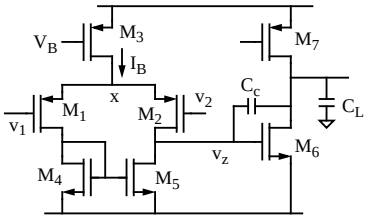


- **Capacitor C across resistor R improves high-frequency performance**
- **Operation:**
  - **If both outputs are high, v_c will go high with respect to v_{ref}.**
  - **v_{bias} will also go high, since the extra amplifier is non-inverting**
  - **M_4 and M_5 will have their current reduced**
  - **The output voltage will be reduced (overall negative feedback)**

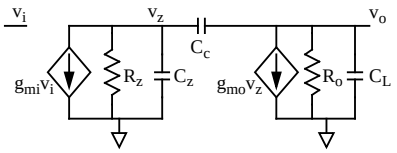
- **summing: use resistors, switched capacitors, transistors in linear region, or differential pair.**
- **resistors across output, or SC can reduce DC gain, however, equivalent R can be very high.**
- **Note: feedback of the appropriate polarity could instead be fed back to M_3 or to M_{10} and M_{11}.**
- **Things to watch out for:**
  - **Stability of CM loop (Tests open loop, or with common-mode step)**
  - **If summing with SC, restricted to time-domain simulations (or replace with R_{eq})**
  - **linearity of sum for large diff voltage**

Two-stage opamp with pole splitting compensation





Small Signal Model



Transfer function: $\frac{v_o}{v_i} \approx A_o \frac{\omega_{p2}\omega_{p2}}{z} \frac{(-s+z)}{(s+\omega_{p1})(s+\omega_{p2})}$

UGBW $= \frac{g_{mi}}{C_c}$, **Slew Rate =** $\frac{I_3}{C_c}$,

Low Freq. gain: $\frac{v_o}{v_i} = \frac{v_o}{v_z} \cdot \frac{v_z}{v_i} = A_o = g_{mo}R_o \cdot g_{mi}R_z$

dominant pole: $\omega_{p1} \approx -\frac{1}{R_z g_{mo} R_o C_c}$

next pole: $\omega_{p2} \approx -\frac{g_{mo}}{C_L}$

RHP zero: $\omega_z \approx \frac{g_{mo}}{C_c}$

Where: $v_i = (v_1 - v_2)$, $g_{mo} = g_{m6}$,
$g_{mi} = g_{m1} = g_{m2}$, $R_z = r_{o2} \| r_{o5}$, $R_o = r_{o6} \| r_{o7}$,
C_z = parasitic (small), C_L = load capacitance

Stability

- **A normal (LHP) zero would add phase lead to improve stability, but RHP zero adds phase lag which reduces stability (45° at ω_z).**
- **Increased load capacitance reduces stability since p_2 moves to lower frequency.**
- **p_2 and z must be beyond UGBW enough so total phase shift due to p_2 and z $< 45°$.**

<u>Rules of thumb</u>: Gregorian and Temes
$|p_2| = |z| = 3$ UGBW $\rightarrow 53°$ **phase margin**

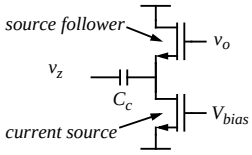
Allen and Holberg $|z| = 10$ UGBW,
$|p_2| = 2.2$ UGBW $\rightarrow 60°$ **phase margin**

Opamp Design: C. Plett

Additions to Pole Splitting, Offsets, Gain Errors, Buffers

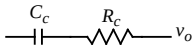
The zero in the RHP can result in instability. Can remove, or compensate for with the following techniques:

1. Buffer, typically source follower, to allow feedback only (removing feed forward)



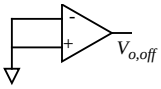
This removes the zero, and the system is left with two poles. These should be separated by the DC gain, or more for stability.

2. Series Resistance

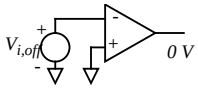


adds $\omega_{p3} = -\frac{1}{R_c C_c}$, **changes** ω_z **to** $\omega_z = \frac{1}{\left(\frac{1}{g_{m6}} - R_c\right)C_c}$, **this allows one to move** $\omega_z \rightarrow \infty$, **or bring it into the LHP where it can cancel out** ω_{p2} **approximately**

Offsets



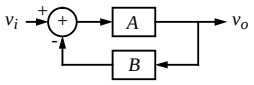
Output referred



Input referred

For gain A,
$V_{i,off} = \frac{V_{o,off}}{A}$

Calculation of Gain Error

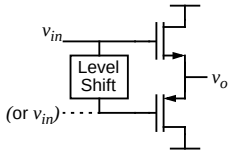


$\frac{v_o}{v_i} = \frac{1/B}{1 + 1/(AB)} \approx \frac{1}{B}\left(1 - \frac{1}{AB}\right)$

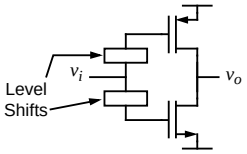
Valid for high A.

Here, desired gain $\approx \frac{1}{B}$, **Gain error** $\frac{1}{AB}$
where AB **= loop gain** $\rightarrow$ **Open loop gain in dB,**
Closed loop gain is $\frac{1}{B}$ **in dB**

Buffers



Source Followers

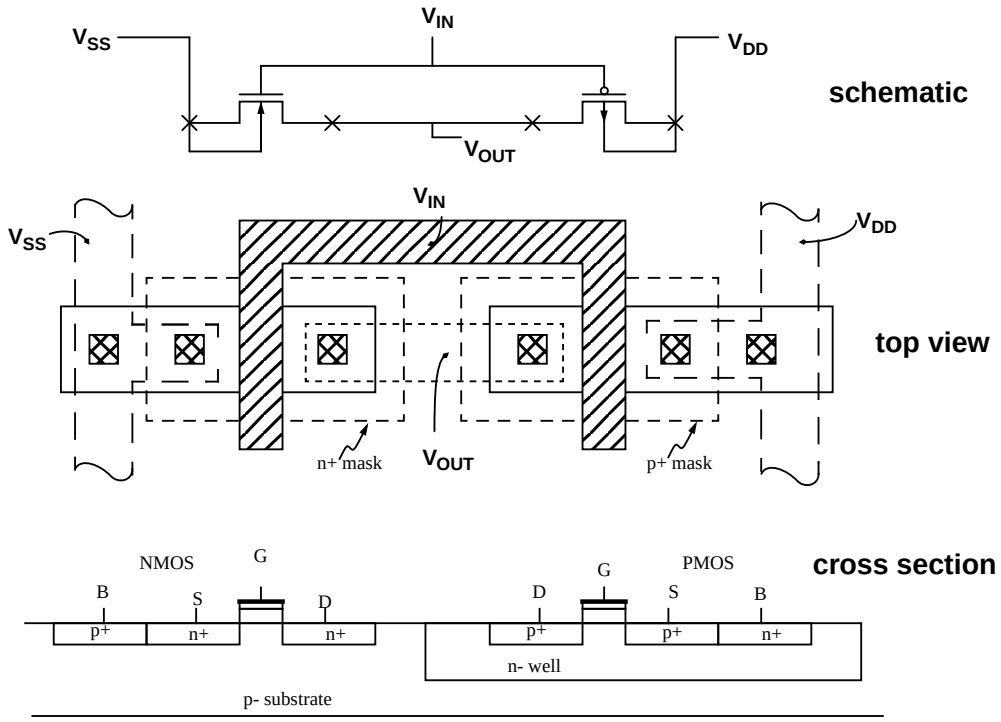


Drain Outputs

- **Source output has low inpedance, limited swing, can only get within V_T from the rails, (assuming v_{in} can go all the way to the rails).**
- **Drain output is a current output, i.e., higher impedance compared to source output, but good swing, can get essentially all the way to the rails.**

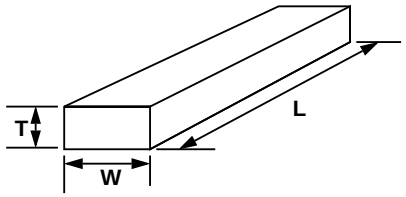
Opamp Design: C. Plett

Layout and Cross Sections of CMOS Transistors (Source - Substrate Connected)



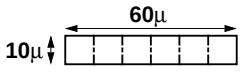
Other Components

Resistors

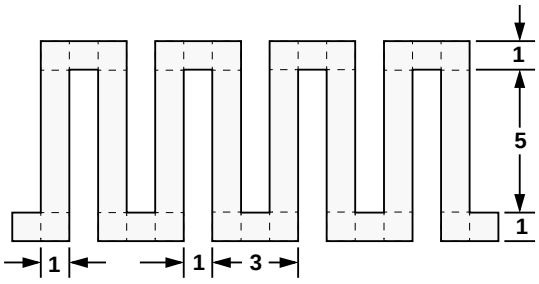


$$R = \rho\frac{L}{A} = \rho\frac{L}{TW} = R_S \cdot \frac{L}{W}$$

- **design information documents often give R_S, the sheet resistance in ohms per square $R_S = \frac{\rho}{T}$. e.g., if $100\Omega/\square$ then $R = 100 \times \frac{60\mu}{10\mu} = 600\Omega$ which we see as 6 squares**



- **a typical resistor:**
  - **in counting total length, corner square is about 0.5 square. Result 57 □ →**



- **Absolute tolerance:**
  - $\approx \pm 20\%$ **for wide resistors** $> 10\ \mu m$
    $\pm 30\%$ for $W = 5\mu m$

- **matching:** $W = 5\mu \pm 3\ \%$, $W = 10\mu \pm 1.2\ \%$, $W = 25\mu \pm 0.8\ \%$, $W = 50\mu \pm 0.2\ \%$

Capacitors

- **Parallel plates of Area A, capacitance per area C_o**

  $C = C_o A$ **where** $C_{ox} = \frac{\varepsilon}{t_{ox}} = \frac{\varepsilon_R \varepsilon_o}{t_{ox}}$.

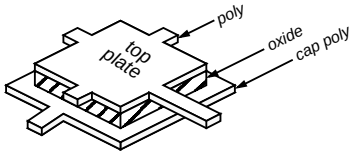
- **if** $t_{ox} = 0.017\mu m$, ε_R **for SiO_2 is 3.9 then**

  $C_{ox} = \frac{3.9 \times 8.854\times10^{-12}(\mathrm{F/m})}{0.017\times10^{-6}(\mathrm{m})} \approx 2\ \frac{\mathrm{fF}}{(\mu\mathrm{m})^2}$ **example:**

  transistor estimate $C_{gs} \approx \frac{2}{3} C_{ox} WL$, **with** $\frac{W}{L} = \frac{150\mu}{1\mu}$

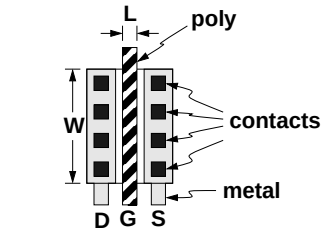
  has $C_{gs} = (2/3) \times 150 \times 2\ (\mathrm{fF}/\mu\mathrm{m}^2) = 0.2\ \mathrm{pF}$.

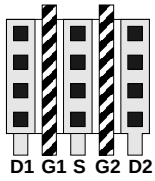
- **capacitors can be metal-metal (MIM), poly-poly or poly-diffusion. (poly-poly shown below)**
- **typically design as multiples of a unit capacitor for best matching, e.g., unit could be 0.5 pF, then could get accurate 1.5 pF match to 2.5 pF.**
- **Otherwise, need to keep area to perimeter ratio the same.**

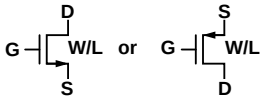


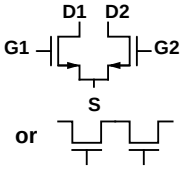
Transistors

- **Often W/L >> 1, so can use multiple contacts for minimal source or drain series resistance**
- **Diagram same for p or n. If PMOS, then in n-well with p+ mask, NMOS in p-substrate with n+.**
- **can have multiple stripes. This can reduce total drain or source area to minimize capacitance.**
- **two gate poly stripes, could be common source, e.g., diff pair, or common connection or since we often cannot tell source and drain apart, it might be a series circuit (for Nand, or cascode).**



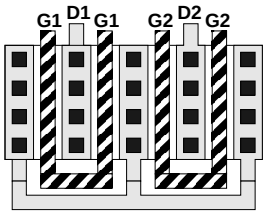


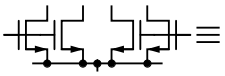


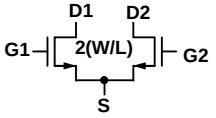


Opamp Design: C. Plett

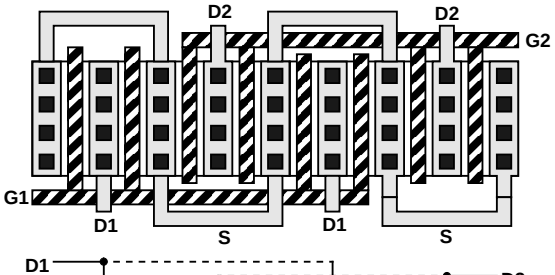
Transistor layout:

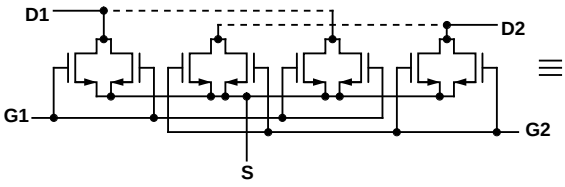


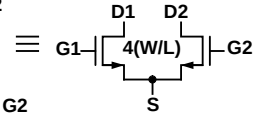




Differential Pair







Common Centroid Differential Pair

Drain connections are not all shown. These missing connections are shown dashed on the schematic below

- **can minimize drain area and perimeter of diff pair to minimize capacitance.**
- **In an opamp, the second (parasitic) pole may be at the drain, so minimum capacitance here can help to increase freq response.**
- **Can interleave two transistors, as in the example above, where there are a total of eight transistors of which four form M1 and four form M2.**
- **This minimizes the effect of process variations and temperature variations across the chip, thus resulting in better matching, and lower offset. This is called the common-centroid topology.**
- **Note: the same interleaving technique can be used for two resistors which need to be matched.**

Opamp Design: C. Plett