CARLETON UNIVERSITY

FINAL
EXAMINATION
December 1997

DURATION 3 **HOURS** No. Of Students 21

Department Name & Course Number: Electronics 97.477
Course Instructor(s): Prof. Calvin Plett

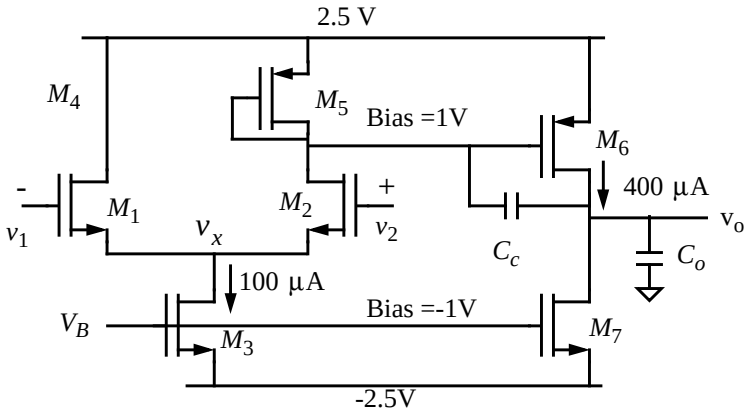
AUTHORIZED MEMORANDA: Official Course Summary and Calculators Allowed

Students MUST count the number of pages in this examination question paper before beginning to write, and report any discrepancy immediately to a proctor. This question paper has 3 pages.

This examination question paper MAY **be taken from the examination room.**

Question 1 (Total 30 Marks)

For the following CMOS Opamp with a diode connected load on the first stage:



$K_{pn} = 100\ \mu A/V^2$

$K_{pp} = 50\ \mu A/V^2$

$V_{TN} = |V_{TP}| = 1\ V$

$\lambda_p = \lambda_n$

$C_c = C_o$

$\gamma_p = \gamma_n = 0$

a) Find the sizes of M_5, and M_6 to result in the bias voltages and currents as shown.

b) Find the transconductances of M_1, M_2 and capacitance values C_c and C_o to result in a UGBW of 5 MHz and a second pole and zero both at 15 MHz. Assume $C_c = C_o$.

c) Find λ_n and λ_p to result in a DC gain of 150. Assume that $\lambda_n = \lambda_p$.

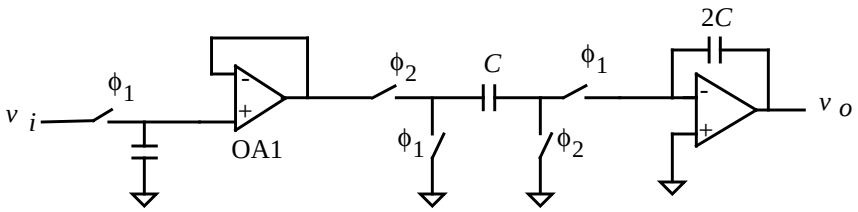
d) Comment on the stability of the opamp in a closed-loop application

e) What is the small-signal voltage v_x for a pure common-mode small-signal input?

f) Assume both inputs are initially at 0V, then the positive input voltage is stepped to 1V. Sketch approximately to scale the transient voltage at the output, clearly showing the slew rate and the final output voltage.

Question 2 (Total 17 Marks)

For the circuit shown below:



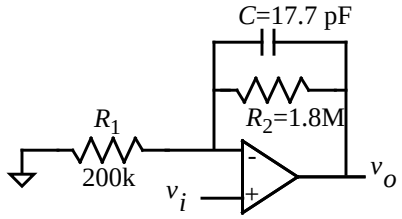
a) Write the Z transform for v_o/v_i. Roughly what is the ratio of the unity-gain frequency f_u to the clock frequency, i.e., what is f_u/f_{clock}?

b) Assume that v_i is a sine wave which is swept from DC up to twice the clock frequency. Sketch the frequency response as seen by a spectrum analyzer. Explain your reasoning.

c) Now suppose the input frequency is fixed at 10/9 of the clock frequency. A spectrum analyzer is used to look at the output signal over the frequency range from DC to twice the clock frequency. Sketch the frequency spectrum as seen by the spectrum analyzer, with approximate relative amplitudes. Explain your reasoning.

Question 3 (Total 18 Marks)

For the following circuit:



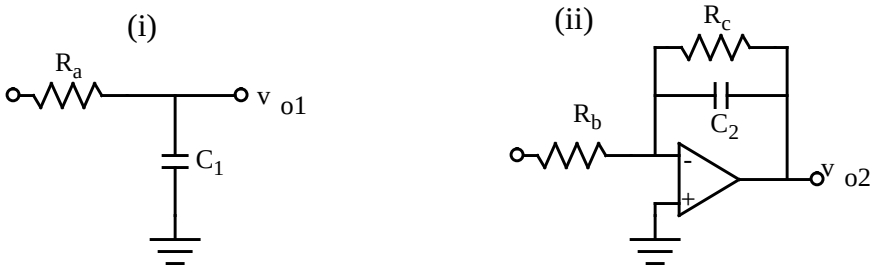
a) Sketch the frequency response showing the low-frequency gain, the high-frequency gain, any poles and zeros, and slopes.

b) Now, if the UGBW of the opamp is 10 MHz, what is the gain error and the corrected gain of v_o/v_i at 200 kHz.

c) Now, if v_i is DC at 0.25 volts, and the DC gain of the opamp is 1000, estimate the common-mode signal at the input of the opamp. What is the difference mode input signal?

Question 4 (Total 17 marks)

We have two different circuits as shown below:

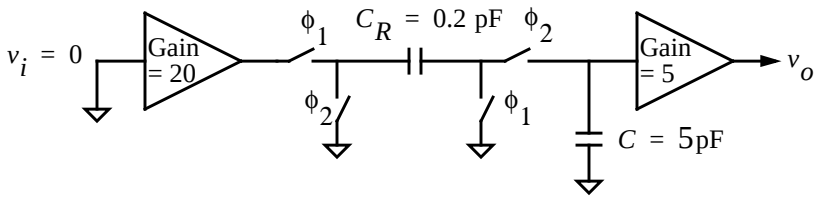


$R_a = R_b = R_c = 500\ \text{k}\Omega$ $C_1 = C_2 = 2\ \text{pF}$

a) Assuming that the only noise is thermal noise in the resistors, what is the total rms noise at the output of circuit (i) relative to circuit (ii)?

b) At 9 kHz, the closed loop circuit in (ii) above has 30 $\text{nV}/\sqrt{\text{Hz}}$ at v_{o2} due to opamp $1/f$ noise. What is the input referred $1/f$ noise in $\text{V}/\sqrt{\text{Hz}}$ at 36 kHz?

c) For the circuit shown below, calculate the rms noise, in volts, at v_o, due to switched capacitor noise.



Question 5 (Total 18 marks)

a) Assume lowpass switched-capacitor filter has unity gain in the passband and a cutoff frequency of 6 kHz and a clock frequency of 156 kHz. Calculate the pole frequency of a unity-gain third-order lowpass anti-alias filter which would reduce the aliasing of the upper replica into the baseband by at least 60 dB. Sketch the filter frequency response. Can the anti-alias filter be a switched-capacitor filter? Explain.

b) Explain the advantages and disadvantages of using a bilinear switched-capacitor integrator instead of the more common integrators as discussed in the course. In a switched-capacitor biquad filter, which integrators are used and why?

c) Explain what design steps can be used to minimize thermal and 1/f noise in a CMOS opamp. How is noise related to power dissipation and layout area? (provide a numerical estimates, if possible, such as: to reduce noise by x requires about y times the power)